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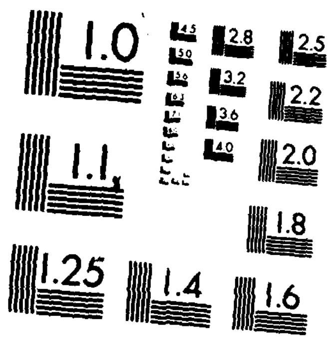

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LATCHUP WINDOW TESTS

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1 February 1983

Technical Report

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This report addresses the very important issue of latchup windows in integrated circuits. This is a serious problem and requires careful consideration in each individual case of system design. Latchup may cause system failure through burnout of the device or through an upset of the circuit in which latchup occurs. The existence of a latchup window was first reported by researchers performing latchup testing of MOS integrated circuits (Refs. 1,2). It was found that latchup would occur in some devices for only a small range of dose rates. At dose rates below a critical value, the device would not

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20. ABSTRACT (Continued)

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1.1 INTRODUCTION

This report addresses the very important issue of latchup windows in integrated circuits. This is a serious problem and requires careful consideration in each individual case of system design. Latchup may cause system failure through burnout of the device or through an upset of the circuit in which latchup occurs.

The existence of a latchup window was first reported by researchers performing latchup testing of MOS integrated circuits (Ref. 1,2). It was found that latchup would occur in some devices for only a small range of dose rates. At dose rates below a critical value, the device would not experience latchup. A second higher dose rate range was found where latchup would again not occur. These tests were performed using high-energy electrons (Linac) and were performed on CMOS, CD4000 series devices.

1.2 PURPOSE OF TESTS

The approach taken to study the latchup window problem is broken into two phases. Phase I constitutes a test program which is to serve as an existence proof. Phase II is designed to study the physical mechanisms which are responsible for the latchup windows. This report describes the series of tests performed in the Phase I program.

1.3 SCOPE OF TESTS

The purpose of these tests is to demonstrate that latchup windows do in fact exist in CMOS devices. Although the previous studies of latchup windows (Ref. 1,2) discovered a number of CMOS devices which apparently had latchup windows, some uncertainties still exist in the minds of many designers. The results were based on the tests performed in a

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1. J. Harrity, "Upset and Latchup Thresholds in CD4000 CMOS Devices," presented at the Annual Conference on Nuclear and Space Radiation Effects, Ithaca, New York, July 1980 (Poster Paper).

2. D. Snowden and J. Harrity, "DNA Support Services," IRT Technical Report IRT 8198-024, October 1980.

single laboratory under a particular experimental set up. The first objective of these tests therefore, is to demonstrate the existence of these windows using an entirely new experimental procedure.

There are a number of secondary objectives to be considered in the latchup window program. One of these addresses the issue of the importance of the existence of a latchup window. Some designers believe that if a device is latchup prone, the device should be discarded or at least circumvented. These kinds of solutions, however, are not always possible; therefore it will be important to determine the scope of the latchup window problem.

A second series of tests was performed on two types of bipolar devices. The tests performed on the bipolar devices were less extensive than those performed on the CMOS parts. To date, no one has reported latchup windows in bipolar devices. Only a few devices were available, and the likelihood of finding a window by a random selection of two types of devices is quite small. Nevertheless, a search for windows in these devices was made.

1.4 REPORT ORGANIZATION

The first part of this report will describe the experimental procedures which were used in these tests. The second part will describe the devices which were used. This will be followed by a summary of the observed data along with some representative presentation of raw data. The report will conclude with some discussion of the data and some of the anomalies observed.

A copy of the test plan used for the Latchup Window tests is included as Appendix A of this report. In addition, a copy of a paper submitted for publication on this topic is included as Appendix B.

2. EXPERIMENTAL PROCEDURES

2.1 FACILITIES

Two linear accelerators were used for the latchup window tests performed in this program. These were: 1) the IRT linear accelerator (LINAC), and 2) the White Sands Missile Range linear accelerator. The IRT facility is ' ıted in San Diego, CA. The White Sands facility is operated by the Nuclear Weap Effects Division of the Army Missile Test and Evaluation Directorate, at the White S ·ıs Missile Range.

2.1.1 IRT Linear Accelerator

The IRT linear accelerator was used in the original experiments which discovered latchup windows (Ref. 1). Therefore, it was important to cross-correlate the equipment and dosimetry used at the two facilities.

The IRT Linac was used for the initial experimental checkout and to prove the correct operation of the circuitry. In addition, all bipolar devices were tested at the IRT Linac.

2.1.2 WSMR Linear Accelerator

The White Sands Missile Range Linac was the principal radiation source for the CMOS latchup window tests. All the CMOS tests were performed during a week-long series of tests at this facility.

The WSMR facility was equipped with a movable table in the exposure area, which made the variation of dose rate quite easy. The facility was also equipped with sophisticated data logging equipment which made data recording extremely convenient.

2.1.3 Operating Characteristics

The operation characteristics of the two Linac facilities are described in References 3 and 4. Some of the more pertinent features of the White Sands Linac are given in the test plan which is included as Appendix A of this report. Both machines were operated at approximately 20 MeV, with a nominal pulsewidth of approximately 70 ns. In actuality, the dose rate range available for tests was greater at the White Sands facility.

2.1.4 Equipment

The IRT Linac facility provided oscilloscopes and some peripheral recording equipment. All transient data and devices were recorded on polaroid film. Dosimetry information and calibration data were provided by the facility.

A variety of measuring equipment was provided by the White Sands test facility. All radiation response data were recorded on Tektronix 7912 transient digitizers. Four channels of data were recorded for each pulse of the Linac, and the pulse shape was monitored using a PIN diode.

2.2 DOSIMETRY

Dosimetry was performed using a PIN diode mounted near the test device package. The PIN response was recorded for each pulse of the Linac and was integrated to provide the dose measurement. The integration was performed automatically by the WSMR computer. The PIN was periodically calibrated against thermoluminescent dosimetry (TLD). The TLD was provided by the White Sands facility and the calibration was made over the full range of expected dose. The resulting calibration curve is shown in Figure 1. The pin diode response shows the expected nonlinearity at higher dose rates. This is caused by the reduced carrier sweepout in the pin diode at high dose rates because of conductivity effects and the reduction of pin diode terminal voltage because of circuit voltage drop.

In addition to the above dosimetry, the primary photocurrent was measured for two 2N2222 devices. These devices were used for measuring correlations and were also measured at the IRT Linac.

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3. Experimenters' Guide for Nuclear Weapons Effects Laboratory at White Sands Missile Range, New Mexico.

4. Tree Simulation Facilities, Second Edition, DNA report DNA2432H, Jan 1, 1979.

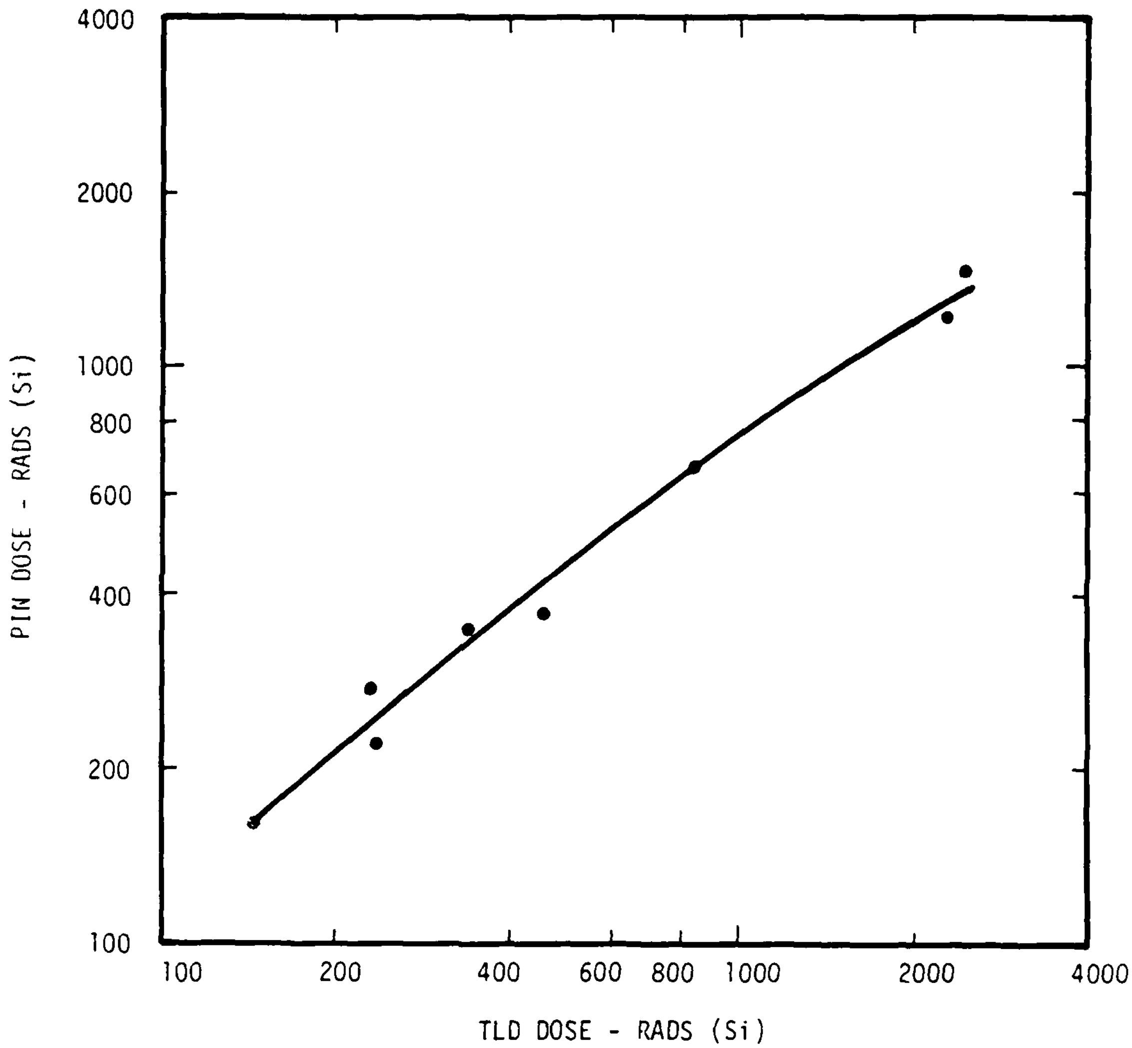

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Figure 1. TLD dose vs. PIN dose

The principal dosimetry used at the IRT facility was a secondary emission monitor (SEM) which provided a m ~sure of the pulse-to-pulse variability of the Linac. The SEM was initially calibrated against gold calorimetry and the resulting correlation data are shown in Figure 2.

2.3 TEST FIXTURE

The original test fixture used in this program was provided by the NWSC, Crane. The fixture had been constructed and used in other test programs by NWSC personnel. this fixture included four line drivers and bias circuitry to provide four data channels. New electronic circuitry described below, was constructed specifically for the latchup window tests, and was incorporated as part of the test fixture. A sketch of this fixture is shown in Figure 3.

2.3.1 Bias Circuitry

The test circuitry used for these tests is shown in the block diagram of Figure 4. This circuit consists of several parts:

1. A threshold detector
2. A control switch and power reset circuit
3. Device interface circuitry
4. Control circuitry
5. Monitor circuitry
6. Timing circuitry.

Each of these will be discussed below.

2.3.2 Threshold Detector

The threshold detector senses the magnitude of the device-under-test power supply current. At a preset time, variable from 1 μs to 500 μs, the circuit determines whether the current is greater than a predetermined threshold current. If the current is greater than the threshold, the circuit initiates action to remove power from the device.

2.3.3 Control Switch and Power Reset Circuitry

At the predetermined delay time, the power supply current is measured. If the power supply current is greater than a preset threshold, power is removed by turning off

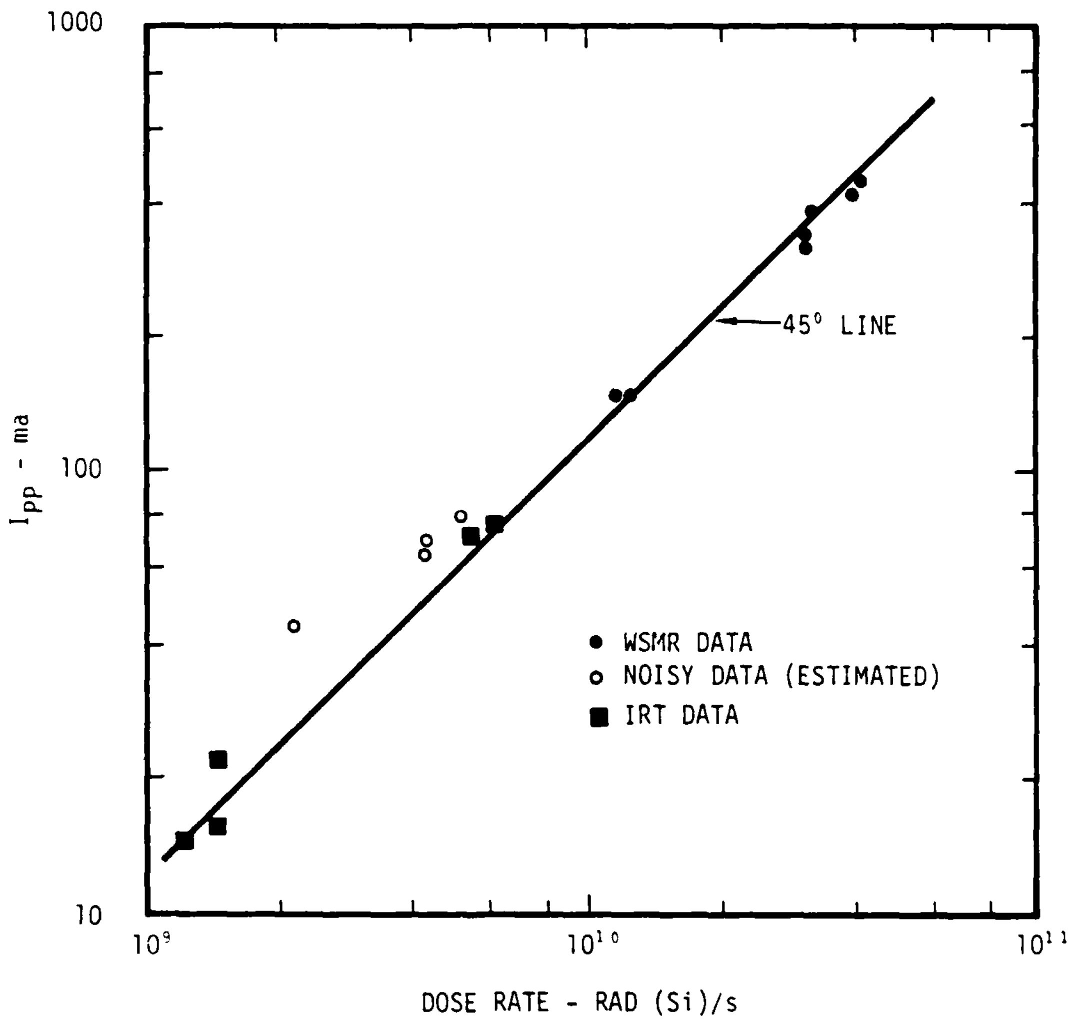

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Figure 2. 2N2222 primary photocurrent data

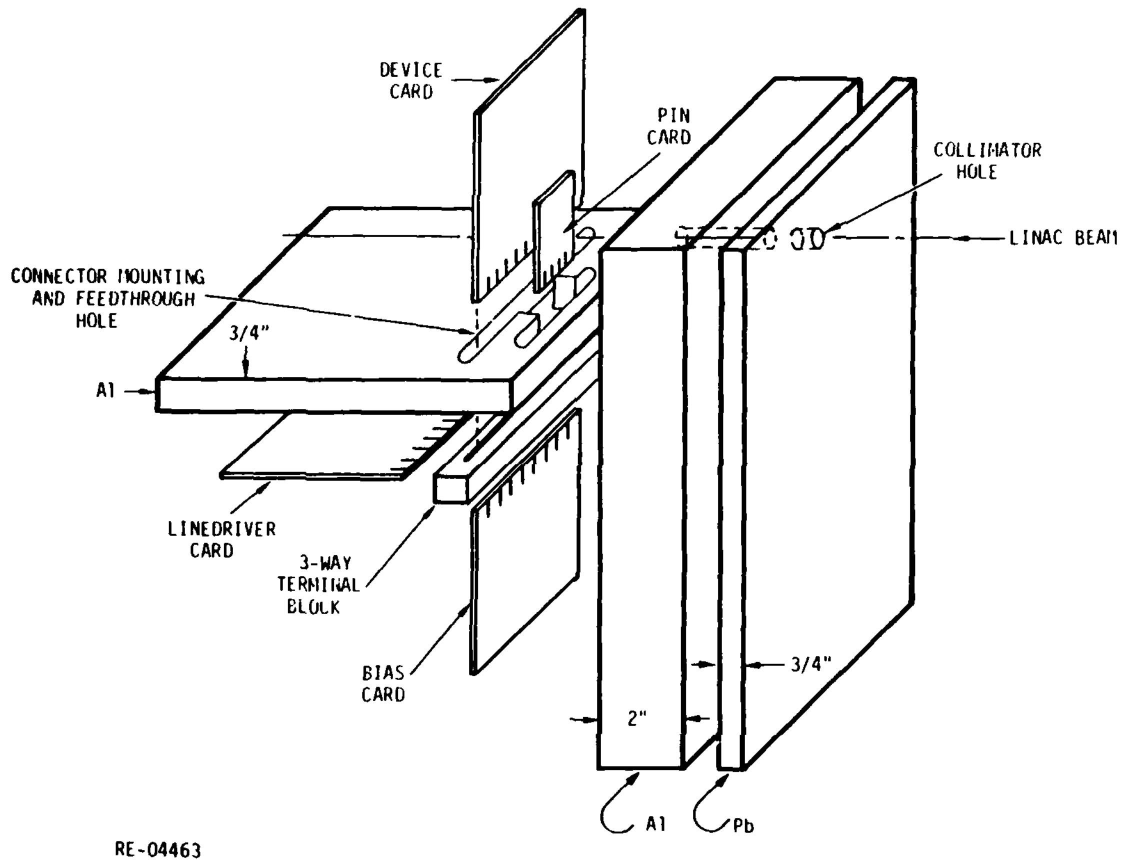

Figure 3. Mechanical layout of test fixture

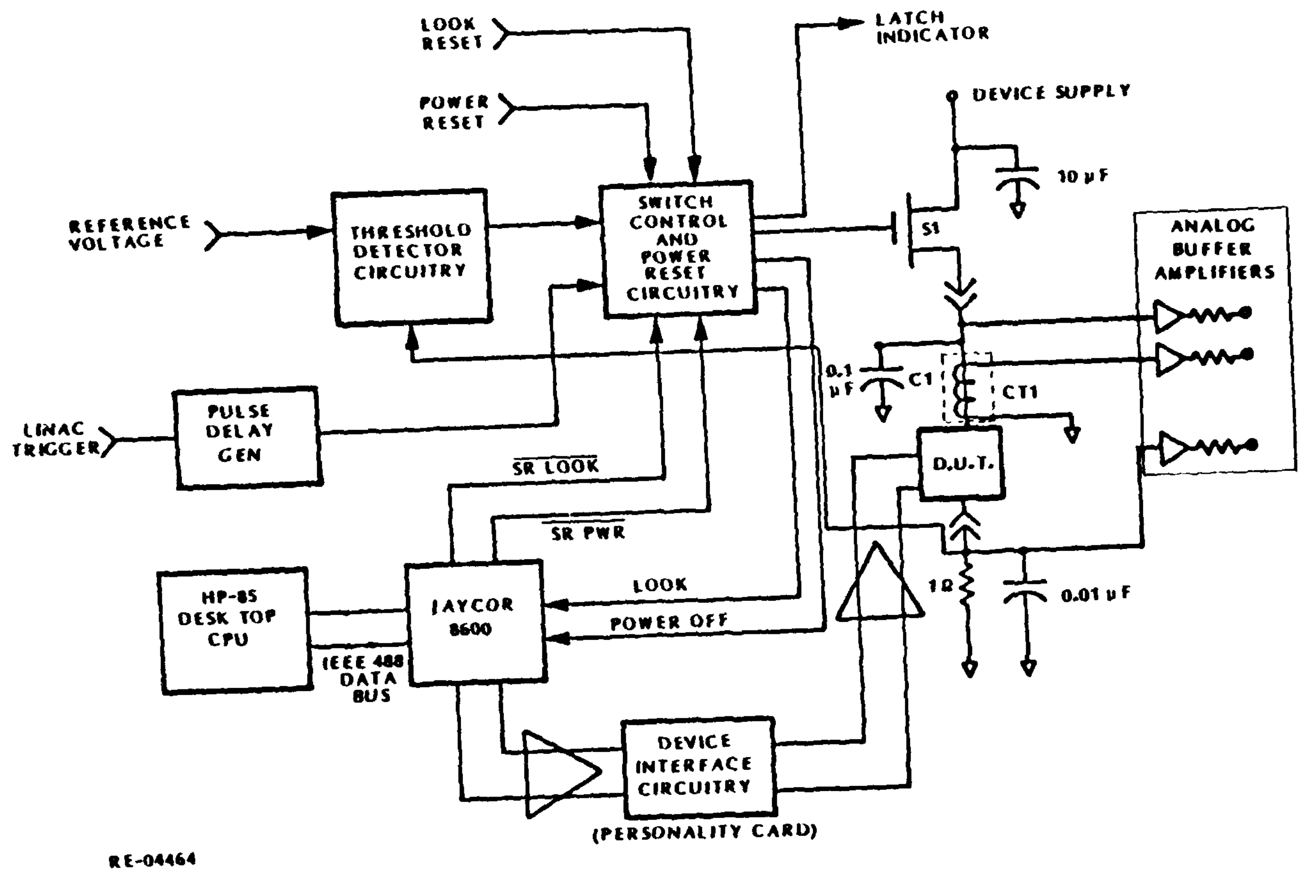

Figure 4. Latchup test system block diagram

the VMOS switch S1. The time required for removing power after the delay time is determined by the capacitor C1, a 0.1 μF capacitor, and the magnitude of the latch current. This time is given approximately by:

$$T = \frac{Q_{C1}}{I} = \frac{V_{C1} \times C1}{I} = \frac{10 \times 0.1 \times 10^{-6}}{I}.$$

For a nominal latch current of 200 mA and a supply voltage of 10 V, the power would be removed in $\sim 5\ \mu s$.

2.3.4 Device Interface Circuitry

The device interface circuitry provides the proper biases and control signals to the device for latchup testing and to exercise the device after the test. Separate 'personality' circuits are constructed for each device type. These circuits interface each individual device with the bias circuitry and controller.

2.3.5 Control Circuitry

The control circuitry consists of an HP-85 desktop computer, which interfaces to the device through a JAYCOR 8600 IEEE bus control/interface unit. This system provides the control to set, reset, and exercise the device for each test. All of the devices were functionally tested and set in a predetermined state before each radiation exposure by use of the circuitry described above and the HP-85 computer.

2.3.6 Monitor Circuitry

The power supply current was monitored using a 1-Ω resistor to sense the current. The 1-Ω resistor is bypassed for fast transients during the ionization pulse. Thus, the resistor monitor measures the long-term latch current should the device latch-up.

A Tektronix CTI current transformer was used to monitor the fast transients during the pulse. In this way, both the fast transients and the steady-state current were monitored.

In addition, the supply voltage at the device power supply input terminal was monitored. In this way, any sag in the supply voltage was easily detected.

2.3.7 Timing Circuitry

Timing for the latchup tests was initiated by the firing of the Linac. The Linac trigger pulse was sensed and used for two purposes. The first was to trigger the recording instruments. The second was to provide a delayed pulse to the power reset circuitry. This was accomplished by applying the trigger pulse to a pulse delay generator, and delaying the pulse for a preset period of time, for which the latch would be allowed to continue. Therefore, if latchup occurred, it would continue until the power was removed and reset by the delayed pulse.

2.4 TEST PROCEDURE

The testing technique to document latchup windows was to irradiate the device under test with at least one pulse at a dose rate below the threshold, and at least two pulses above the threshold for latchup, but within the window. This procedure demonstrated that the latch condition was repeatable. Then at least two pulses were required above the latchup window range to demonstrate clearly that no latchup occurred at the higher dose rates. Finally, another pulse was taken within the latchup window range to assure that the window still remained after all the previous testing.

2.5 DEVICES

The principal effort in this program was to test CMOS devices and to verify the existence of latchup windows in these devices. The types which were tested were the CD4047 multivibrator, the CD4061 memory and the CD4094 shift register. These types were chosen for test because previous work (Refs. 1 and 2) had reported latchup windows in these devices. The bias circuitry used for these devices is shown in Figures 5, 6 and 7.

In addition to the CMOS tests, a limited number of bipolar devices were tested. These were the 54LS138 decoder and the AD580S regulator. These devices were chosen because of availability and because latchup had been reported in these types. The bias circuitry used for these tests is shown in Figures 8 and 9.

The nominal bias voltage (V_{DD}) for the CMOS devices was 10 volts. This voltage was deliberately varied in order to observe any bias dependencies of the latchup phenomenon. The nominal voltage for the bipolar devices is shown in the figures.

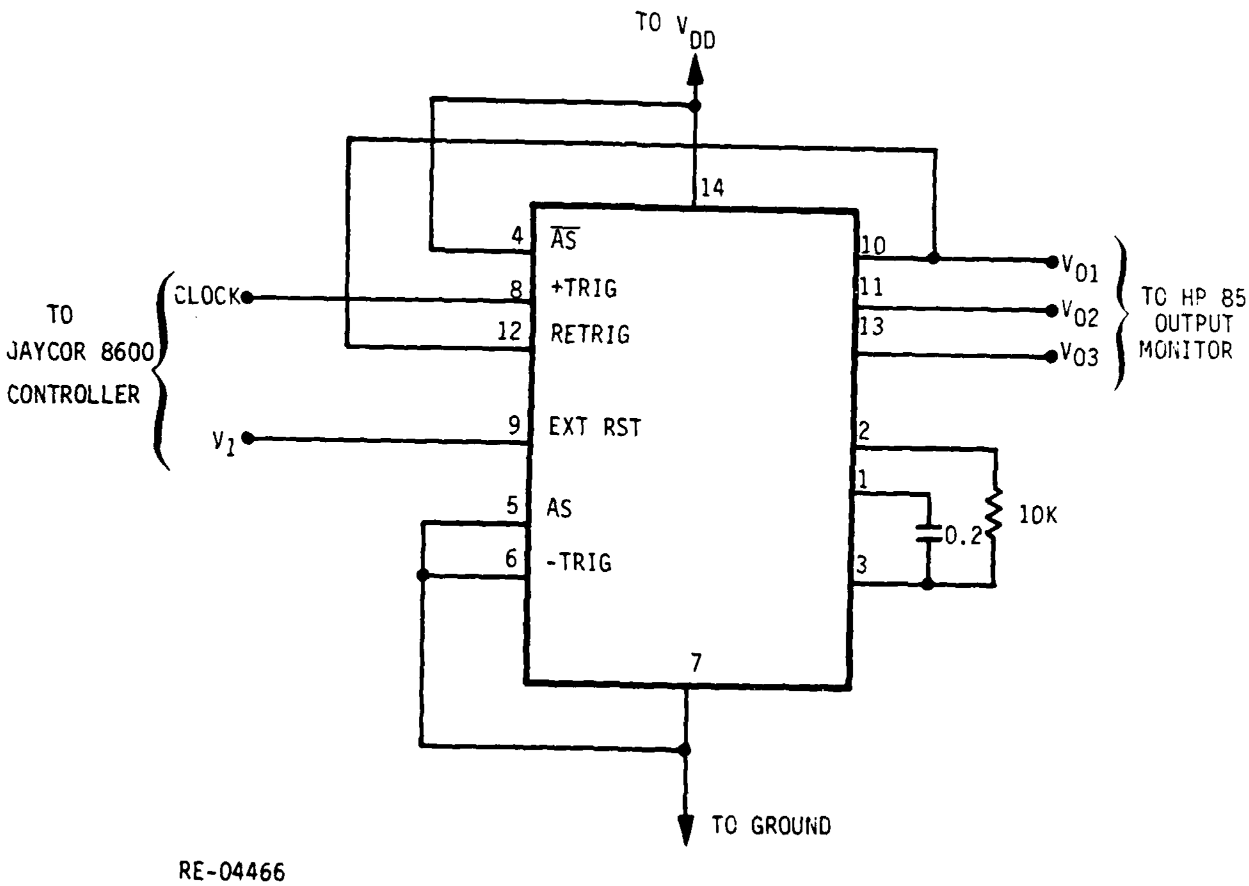

Figure 5. Bias circuit and test circuit for the CD4047 multivibrator

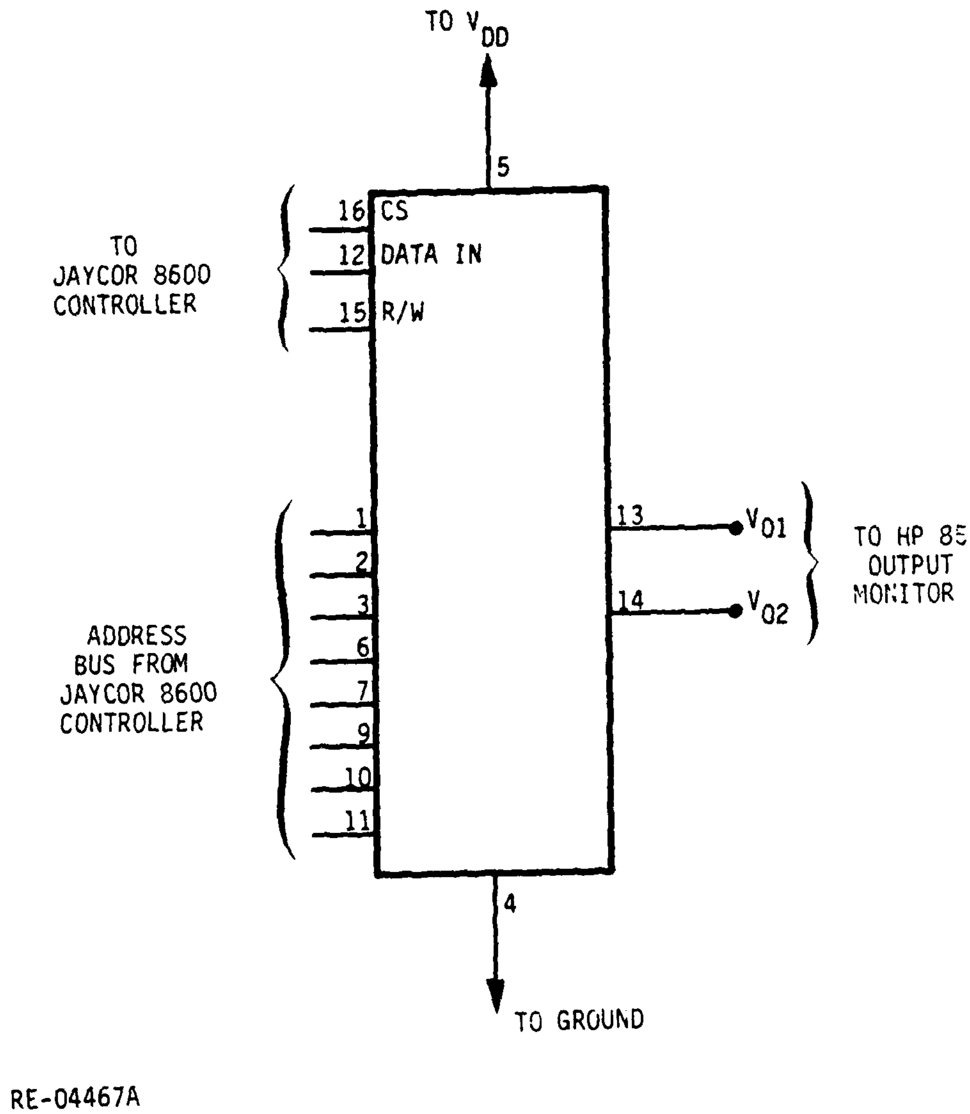

Figure 6. Bias and test circuit for the CD4061 static RAM

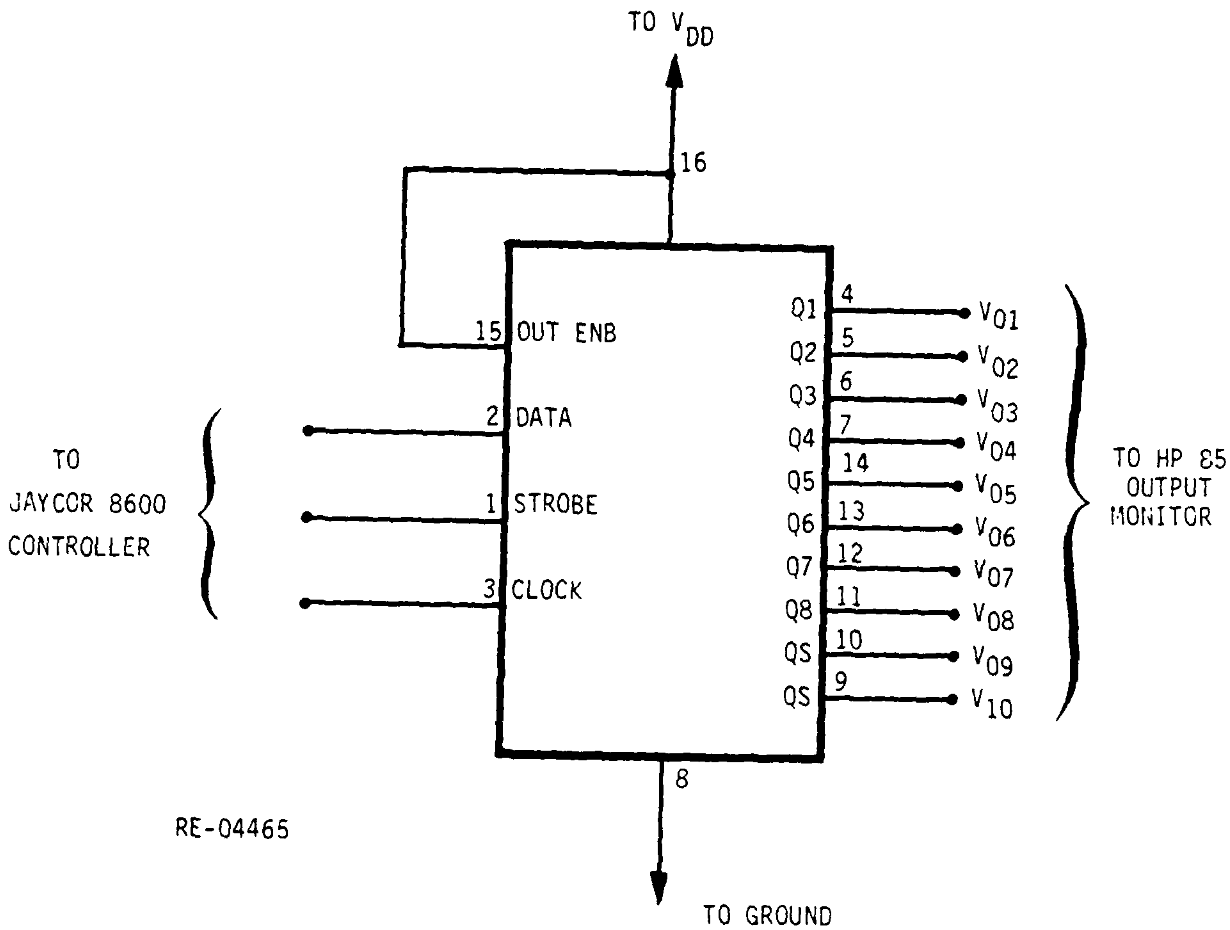

Figure 7. Bias and test circuit for the CD4094 shift register

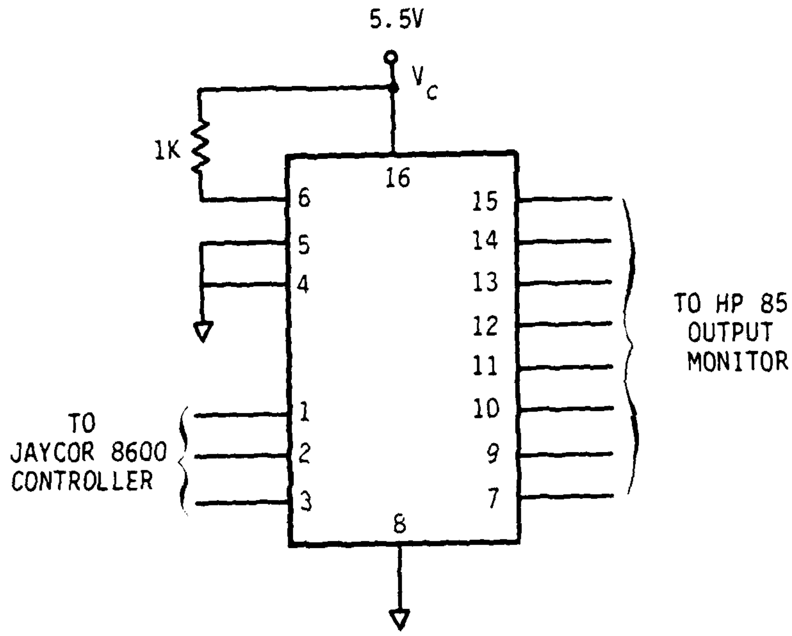

Figure 8. Bias and test circuit for the 54LS138 line decoder

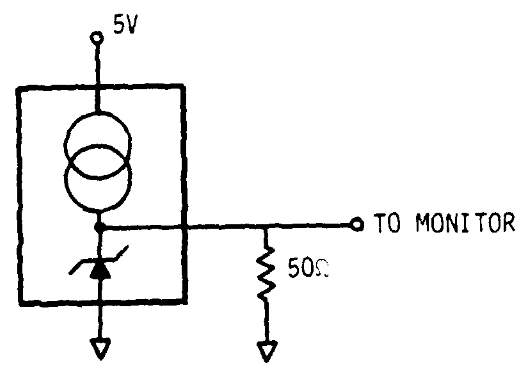

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Figure 9. Bias and test circuit for the AD580S regulator

3. DEVICES

3.1 INTRODUCTION

Although a considerable effort was made to acquire test devices from system houses which had conducted government-sponsored latchup programs, only a few devices were able to be collected. Therefore, the first tests were made strictly on CMOS devices, which were available from previous DNA programs.

3.1.1 CMOS Test Devices

The CMOS devices which were available for these tests are shown in Table 1. All the devices were RCA CD4000-series devices; however, the source and pedigree of the devices did change. The table shows the device type, the number available and the controlling organization which acquired the devices.

The tests for latchup windows proved to be quite time consuming. Several pulses were required to characterize the device correctly; therefore, a considerable amount of facility time was required to test each device. As a result, it was not possible to test all the available devices. The priorities for these tests were to first test those devices which had previously been reported to have a latchup window in order to verify the existence of the window.

The second priority was to test new devices acquired from Sandia. These devices were similar to the devices which had already exhibited latchup windows.

Finally other devices were tested as time permitted. In all, approximately 39 devices were tested and of these 39, 17 exhibited the latchup window phenomenon. A brief summary of these results is given in Table 2.

3.1.2 Bipolar Test Devices

A search was made for suitable bipolar test vehicles to use in the program. There was limited success and very little cooperation from systems houses. However, with the assistance of DNA, a few devices were acquired from one system. These devices were:

8 - 54LS138 decoders

4 - AD580S regulators.

Table 1. CMOS devices on hand for latchup window program

Device Type	Number	Date Code	Source	Remarks
CD4047A	[illegible]	7709	IRT	Original source was Sandia
CD4047AD	20	923	IRT	Commercial purchase
CD4047BE	20	127	JAYCOR	Commercial purchase
CD4047AE	20	127	CRANE	Commercial purchase
CD4061AD	24	7652	IRT	Original source was Sandia
CD4061AD	5	7651	SANDIA	--
CD4061AD	20	049	JAYCOR	Commercial purchase
CD4094A	18	7939	IRT	Original source was Sandia
CD4094A	9	719	IRT	Commercial purchase
CD4094BD	21	923	IRT	Commercial purchase
CD4094BE	20	123	JAYCOR	Commercial purchase
CD4094A	5	7705	SANDIA	--
CD4094BE	20	127	CRANE	Commercial purchase

Table 2. Summary of latchup window results

Type	Number tested	Source	Latchup window	Previous window
CD4047	3	IRT	1	0
	2	JAYCOR	0	0*
	3	SANDIA	2	2
CD4061	5	IRT	5	5
	2	JAYCOR	0	0*
	4	SANDIA	4	0*
CD4094	10	IRT	3	7
	4	JAYCOR	0	0*
	3	CRANE	0	0*
	3	SANDIA	2	0*
54LS138	5	SYSTEM	2	0*
AD580S	2	SYSTEM	0	0*

*Not previously tested.

These devices were of interest because they had all failed a latchup screen test at a Linac facility. In a repeat of the latchup screen at a flash x-ray (FXR705), the devices all passed the screen; the apparent latchup at the Linac was blamed on long recovery time. Since the dose rate used at the FXR latchup screen was different from the dose rate used at the Linac, these devices made good candidates for latchup window tests.

These bipolar devices were then retested as part of the JAYCOR latchup window program. Five of the 54LS138 devices and two of the AD580S regulators were tested at the IRT Linac facility. The experiment was successful in finding latchup in the 54LS138, but definite evidence of a latchup window was not found. However, in reducing the data on the 54LS138, one of the devices, where a significant number of pulses were taken, had anomalous results, which will be described later.

Tests on the AD580S were inconclusive. No latchup was attained; however, the test configuration differed considerably from previous tests.

3.2 TYPICAL DATA

The experimental technique used to detect latchup used a number of different *measurements. These were:*

1. Computer detection of latchup
2. Measurement of power supply current
3. Measurement of supply voltage
4. Measurement of PIN signal.

3.2.1 Computer Detection

The computer system was designed to:

1. Exercise the device prior to the test,
2. Detect a high power supply current at a preset time and remove power,
3. Exercise the device to determine if the latchup caused any damage.

Figure 10 shows an example of the computer output after a device check. Notice that a record of the device type and serial number is recorded as well as the Linac pulse number. The reference voltage is the preset value of voltage which sets the current level which initiates the voltage shutdown circuit. In this case, the voltage reference of 0.3 volts will cut off the power if the device current sustains a value of 30 mA.

```
************************************
TEST DEVICE               CD4094B
DATE LOT CODE             IRT DEVICE
DEVICE SERIAL #           P-2
SHOT NUMBER               124
REF VOLTAGE               0.30

HAVE LATCH UP


ALTERNATE 1'S & 0'S TEST

   QS Qs Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1
SB 0  0  0  1  0  1  0  1  0  1
IS 0  0  0  1  0  1  0  1  0  1
ER


PLUS 1 CLOCK

   QS Qs Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1
SB 1  1  1  0  1  0  1  0  1  0
IS 1  1  1  0  1  0  1  0  1  0
ER


STROBE OFF + 1 CLK

   QS Qs Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1
SB 0  0  1  0  1  0  1  0  1  0
IS 0  0  1  0  1  0  1  0  1  0
ER


STROBE ON

   QS Qs Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1
SB 0  0  0  1  0  1  0  1  0  1
IS 0  0  0  1  0  1  0  1  0  1
ER

NUMBER OF ERRORS =  0


END OF TEST
```

Figure 10. Example of HP-85 computer output after a latchup event

The particular device check shown in Figure 10 has a latchup indication. The test sequence after interrupting power to remove latchup indicates that the device is still functional.

3.2.2 Power Supply Current

Figure 11 shows the Tektronix transient digitizer 7912 output for the power supply current. The upper trace is the device current displayed on a long time scale, 10 μs/div. This current is monitored across a 1-Ω resistor shunted by a 0.01 μfd capacitor.

For fast transients (early time data) the device current is also monitored with a CTI current transformer. This is shown in the lower trace of Figure 11.

The device has latched and continues to conduct 200 mA supply current for 90 μs. At this point power is removed and latchup terminates.

3.2.3 Power Supply Voltage and Dose

Figure 12 shows the Tektronix 7912 output for the PIN signal and the device supply voltage. The upper trace is the PIN output along with the reduced data printout for the dose. The dose is the uncorrected value and must be corrected for PIN non-linearities.

The lower trace is the device supply voltage. There is a slight dip in the voltage (~ 0.6 v) during the prompt photocurrent conduction, caused by ohmic drops in the circuit. The voltage holds steady until 90 μs when the power is removed.

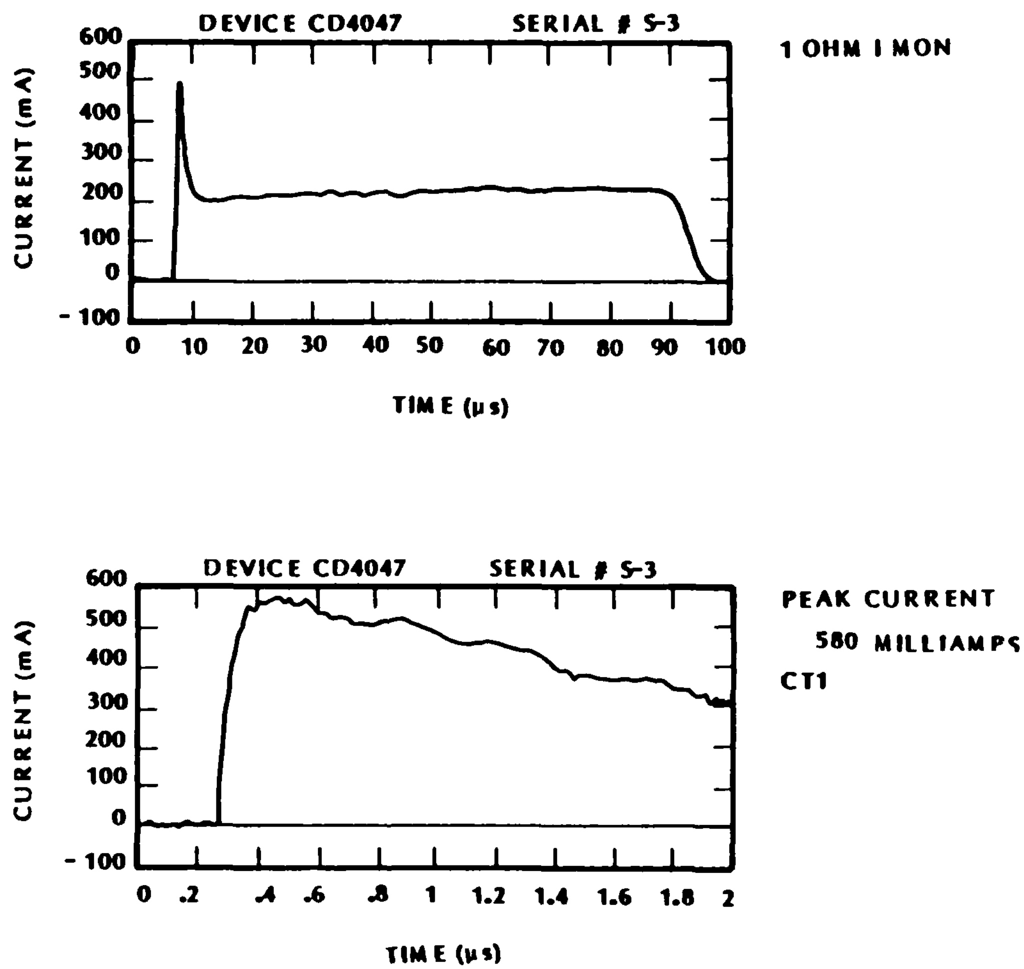

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Figure 11. Typical supply current monitor output

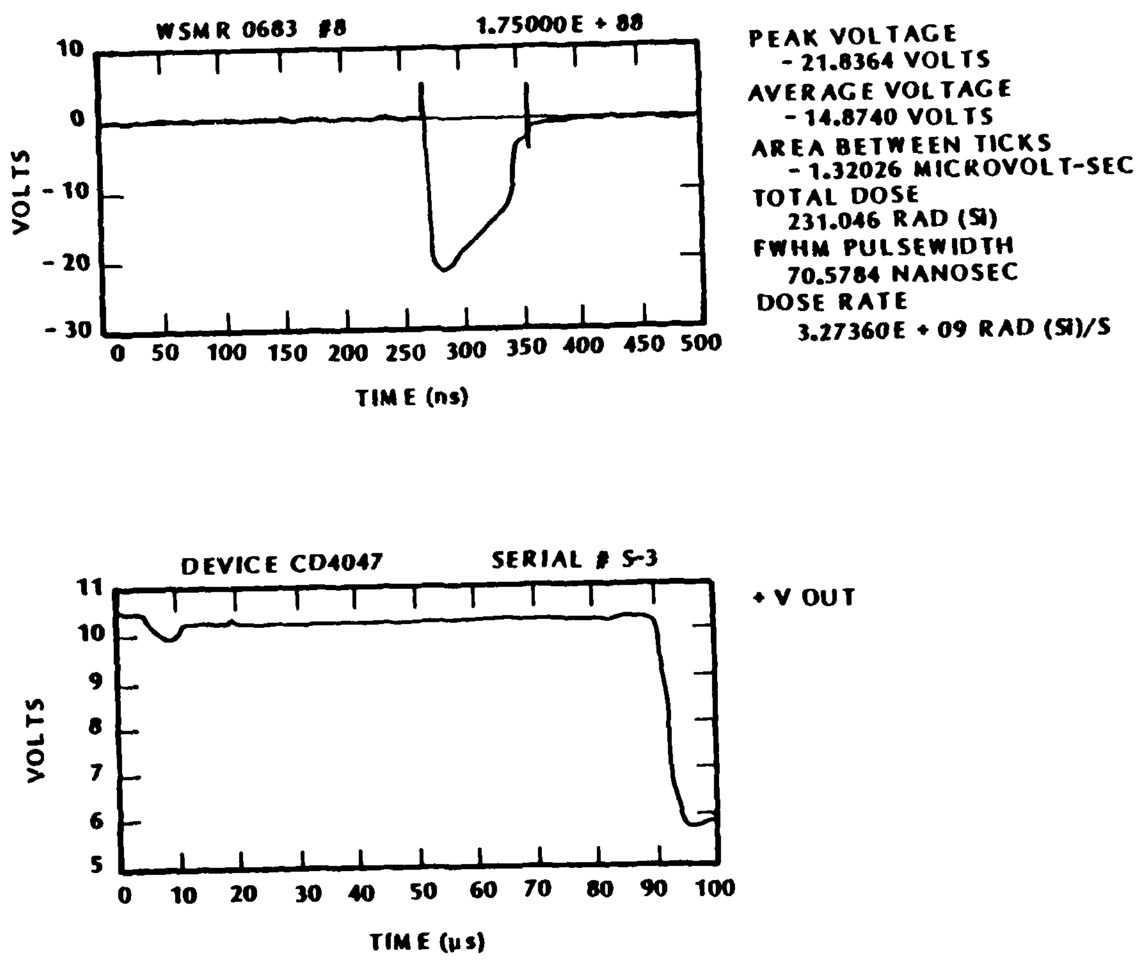

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Figure 12. Typical PIN and supply voltage monitor output

4. DATA

4.1 GENERAL

This section will present typical data demonstrating the existence of latchup windows. In the course of the tests, data were taken at doses below the latchup window threshold, data for at least two pulses within the window, additional data for at least two pulses at doses above the window and a final pulse within the window. In this way, data is taken for a minimum of three pulses showing latchup within the region of latchup, and at least two pulses showing no latchup at higher dose levels.

The long term conduction current will be presented in this section as evidence of latchup. One should keep in mind that all data of the type described in section 3.3 are available for each pulse.

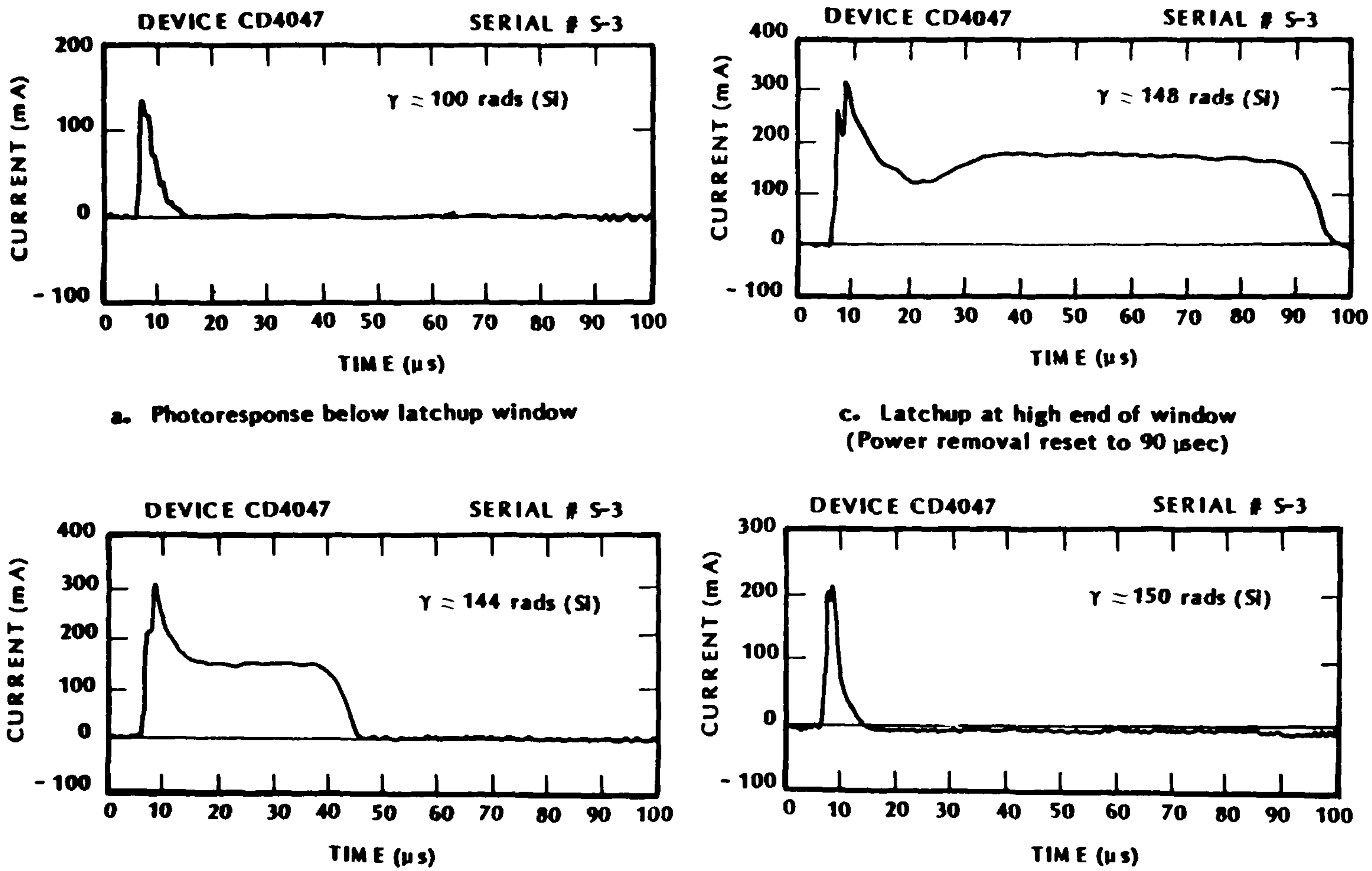
4.2 CD4047 DATA

Figure 13 shows the latchup window behavior of the CD4047A, CMOS multivibrator. These data were taken with the supply voltage at 10 volts. The threshold for latchup occurred between 100 and 144 rads (Si).

The actual latchup is shown in Figure 13b. In this case, the supply voltage was removed at 40 μs, terminating the latchup. We clearly see a latchup window, since the latchup condition in Figure 13 is bracketed by a higher and a lower dose rate point.

Table 3 summarizes the latchup results for all the CD4047 devices which were tested in this program. The CD4047 devices tested in Ref. 2 were not reported to have latchup windows in that program; however, two windows were discovered in these same devices in the new tests. Another important point to note is that a window was created by slightly lowering the voltage (0.2 V) supplied to the device CD4047AD-C18. No window was found at the higher voltage.

The thresholds for latchup are compared to the values previously obtained in Ref. 2. These are shown in parentheses in the table.



a. Photoresponse below latchup window

c. Latchup at high end of window (Power removal reset to 90 μsec)

b. Latchup at low end of window

d. Photoresponse above latchup window

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Figure 13. Latchup window behavior for the CD4047-CMOS multivibrator, V_{DD} ≈ 10 V, PW ~70 ms (CD4047A, Lot 7709)

Table 3. Summary of latchup window results for CD4047 devices

Device	Lot	Serial	V_{DD} supply volts	Window	Dose range for latchup threshold R (Si)	Dose range for no latchup threshold R (Si)	Prompt current mA	latchup current mA
CD4047AD	7709	S1	10	yes	132 - 133 (155 - 185)	133 - 135	340	140
CD4047A	7709	S2	10	no	148 - 173 (150 - 180)	-	626	200
CD4047A	7709	S3	10	yes	100 - 144 (105 - 150)	149 - 150	352	150
CD4047BE	127	J1	10	no	- 124	-	500	525
CD4047BE	127	J2	10	no	61 - 65	-	395	600
CD4047AD	923	C18	10	no	206 - 257 (195 - 215)	-	400	190
			9.8	yes	257 - 278	851 - 870	400	190
CD4047AD	923	C22	10	no	212 - 268 (150 - 155)	-	400	190
CD4047AD	923	C24	10	no	139 - 271 (155 - 180)		420	180

Note:
1) The two values for each threshold indicate the range in which the threshold occurs.
2) The values in parentheses are the values previously attained in Reference 2.
3) The currents are given for the lowest dose where latchup has occurred.

4.3 CD4061 DATA

Figure 14 shows the typical response of the CD4061 to the Linac pulses. These data were taken with the supply voltage nominally at 10 volts. In some cases, the voltage was varied in order to observe any bias dependency of the latchup window. The latchup occurred between 12 and 20 rad(Si).

The actual latchup is shown in Figure 14b. In this case, the supply voltage was removed at about 50 μs, terminating the latchup. These data clearly indicate a latchup window, since the latchup was bracketed by a higher and lower dose point.

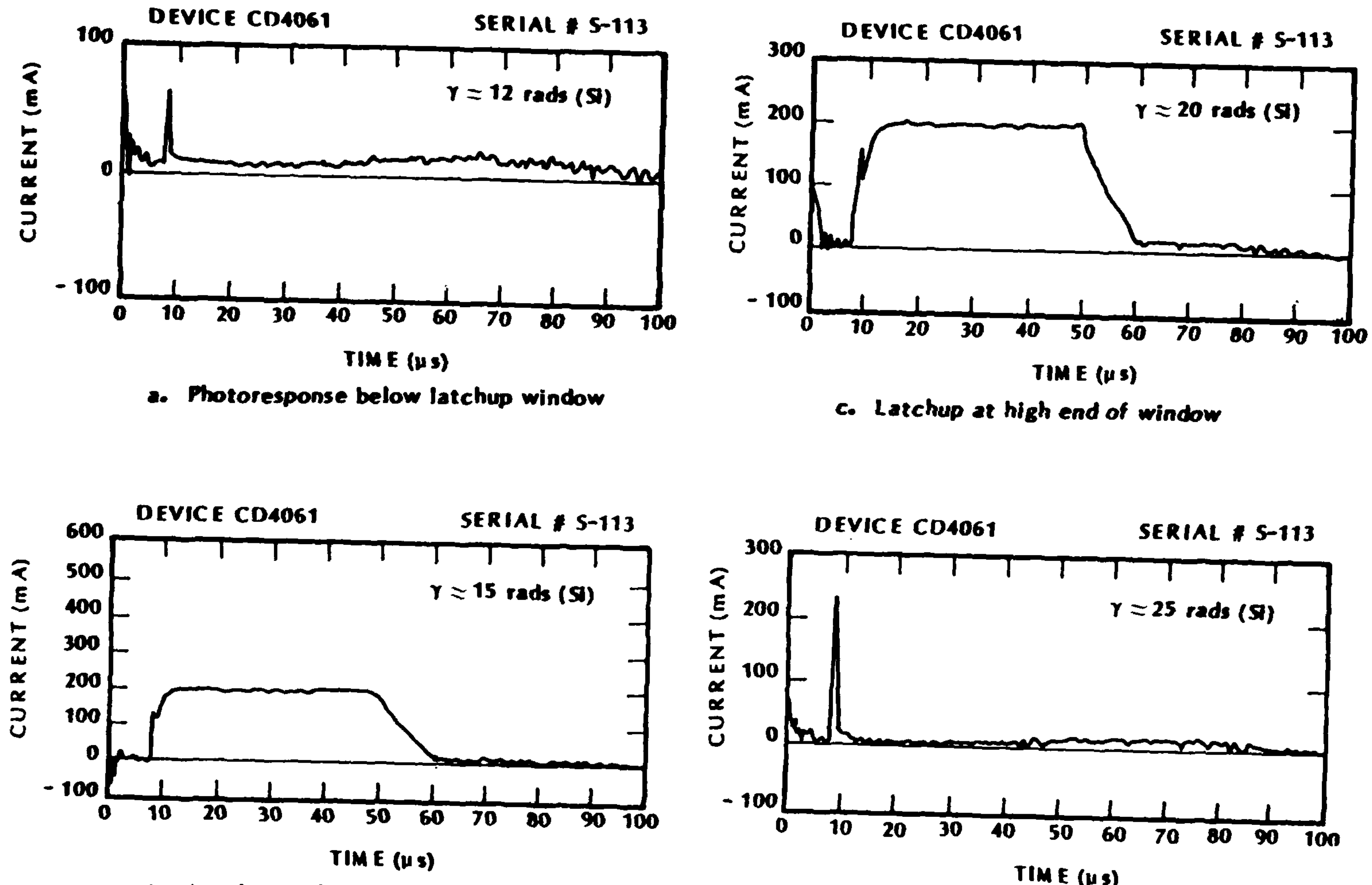
Table 4 summarizes the results for all of the CD4061 RAMs which were tested. There is good agreement between the devices tested in Ref. 2 and these results. It is again interesting to note, that in two of the devices, I1 and I2, a latchup window was created by lowering the device voltage. For example, a window was not seen in device I1 at 10 volts; however, at 7.5 volts, a window was in fact found.

4.4 CD4094 DATA

Figure 15 shows the typical response of the CD4094 shift register to the Linac pulses. These data were taken with the supply voltage nominally at 10 volts, and this figure once again indicates the typical latchup window response.

Table 5 summarizes the results for all of the CD4094 devices tested in this program. The agreement between these results and those obtained previously (Ref. 2) is not as good as might be expected. This particular device seemed to be extremely sensitive to voltage and temperature variations. In fact, at the outset, the latchup window could not be reproduced on repeated tests made on different days of the test. It was decided however, that tests at a slightly higher supply voltage might offset the effects of lower temperature. A change of 0.2 volts did in fact accomplish the objective. Once the voltage was raised slightly, the windows were reproduced.

Some of the early data listed in the table were taken before it was decided to vary the applied voltage. Hence, the results may not totally reproduce those of Reference 2 on devices common to both sets of tests. Slight variations in temperature and voltage may account for these discrepancies.



a. Photoresponse below latchup window

c. Latchup at high end of window

b. Latchup at low end of window

d. Photoresponse above latchup window

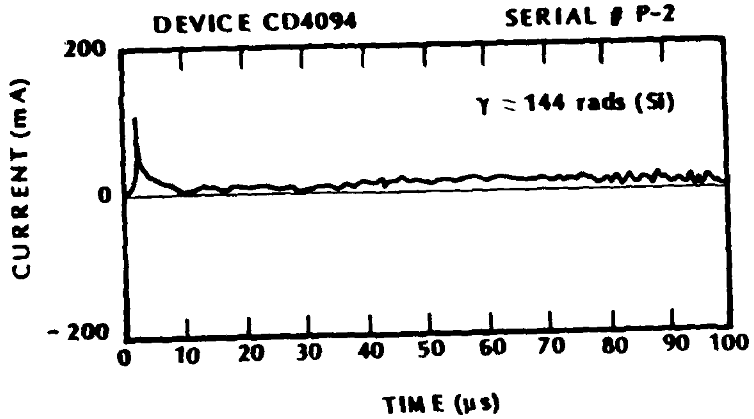
RE-04667

Figure 14. Latchup window behavior for the CD4061-CMOS RAM, $V_{DD} \approx 10$ V, PW ~70 ms (CD4061AD, Lot 049)

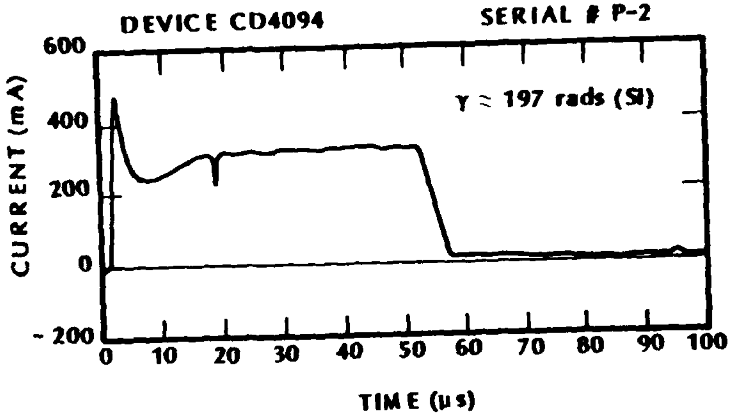
Table 4. Summary of latchup window results for CD4061 devices

Device	Lot	Serial	V_{DD} supply volts	Window	Dose range for latchup threshold R (Si)	Dose range for no latchup threshold R (Si)	Peak current mA	latchup current mA
CD4061AD	7652	I1	10.0	no	5 - 10 (10 - 11)	-	170	210
			8.6	yes	5 - 16	18 - 23	216	195
			7.5	yes	12 - 15	15 - 19	196	150
CD4061AD	7652	I2	10.0	no	11 - 13 (9 - 10)	-	168	200
			8.4	yes	11 - 13	17.9 - 18.4	228	180
CD4061AD	7652	I6	10.4	yes	13 - 16 (12 - 15)	21 - 29 (20 - 27)	209	200
CD4061AD	7652	I11	10.4	yes	12 - 15 (12 - 14)	21 - 24 (31 - 38)	211	200
CD4061AD	7652	I23	10.4	yes	13 - 15 (12 - 16)	18 - 26 (31 - 34)	212	200
CD4061AD	049	J2	10.4	no	-	-	-	-
CD4061AD	049	J4	10.4	no	-	-	-	-
CD4061AD	7651	S112	10.4	yes	12 - 16	20 - 27	220	200
CD4061AD	7651	S113	10.2	yes	12 - 15	20 - 25	216	200
CD4061AD	7651	S114	10.4	yes	14 - 15	18 - 19	213	200
			10.2	yes	15 - 17	17 - 17.5	236	200
CD4061AD	7651	S115	10.2	yes	14 - 16	18 - 21	231	200

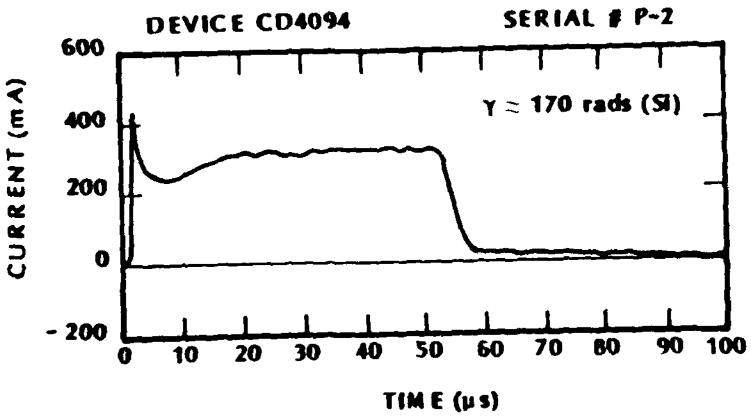
Note: 1) The two values for each threshold indicate the range in which the threshold occurs.
2) The values in *parentheses* are the values previously attained in Reference 2.
3) The currents are given for the lowest dose where latchup has occurred.



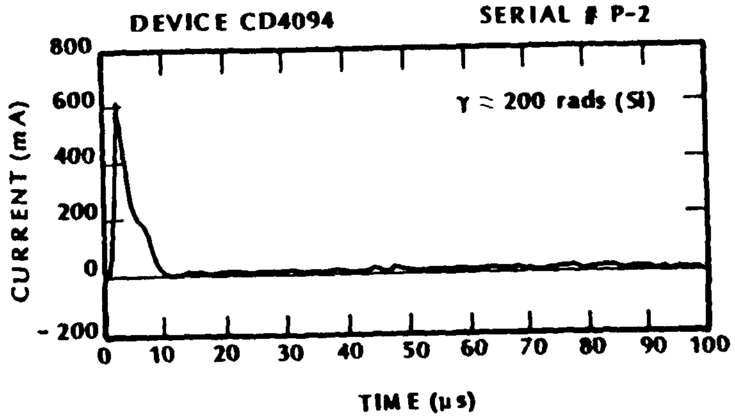
a. *Photoresponse below latchup window*



c. Latchup at high end of window



b. latchup at low end of window



d. Photoresponse at high end of window

Figure 15. Latchup window behavior for the CD4094-CMOS shift register, $V_{DD} \approx 10$ V, PW ~70 ns (CD4094BD, Lot 923)

RE-04666

Table 5. Summary of latchup window results for CD4094 devices

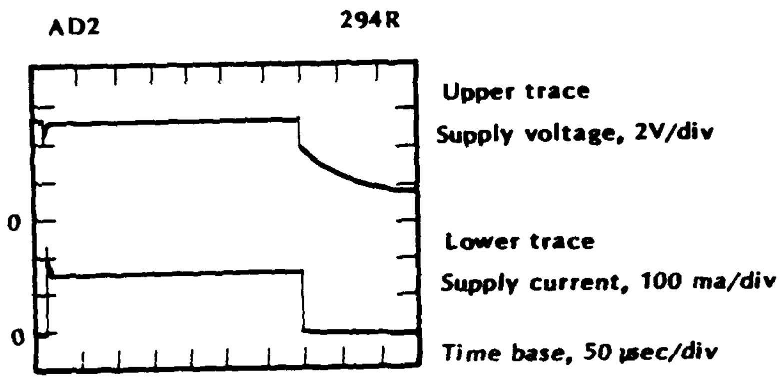
Device	Lot	Serial	V_{DD} supply volts	Window	Dose range for Latchup threshold R (Si)	Dose range for no latchup threshold R (Si)	Peak current mA	latchup current mA
CD4094BD	719	P1	10	no	- (110 - 135)	- (135 - 155)		
CD4094BD	719	P2	10	yes	144 - 170 (140 - 145)	197 - 200 (160 -)	700	300
CD4094BD	719	P4	10	no	-	-		
CD4094BD	719	P5	10	no	- (135 - 150)	- (1200 - 1250)		
CD4094BD	719	P6	10	no	- (135 - 150)	- (1200 - 1250)		
CD4094BD	719	P7	10	yes*	321 - 374 (340 - 370)	643 - 768 (395 - 410)	1400	300
CD4094BD	719	P8	10	no	-	-		
CD4094BD	719	P9	10	no	- (245 - 265)	- (720 - 745)		
CD4094BE	123	J1	10.4	no	-	-		
CD4094BE	123	J2	10.4	no	-	-		
CD4094BE	123	J3	10.4	no	-	-		
CD4094BE	123	J4	10.4	no	-	-		
CD4094BD	7939	I4	10.2	no	-	-		
CD4094A	7939	I24	10.2	yes	401 - 403 (345 - 375)	407 - 418 (490 - 550)	965	400
CD4094BE	127	CR1	10.4	no**	?			
		CR2	10.4	no	?			
		CR3	10.4	no**				
CD4094A	7705	S2	10.4	yes	145 - 208	828 - 1030	965	400
CD4094A	7705	S3	10.4	yes	215 - 329	579 - 600	955	400
CD4094A	7705	S4	10.2	no	144 - 210		750	410

*This device had multiple windows in this range.
**This device had incipient latchup.

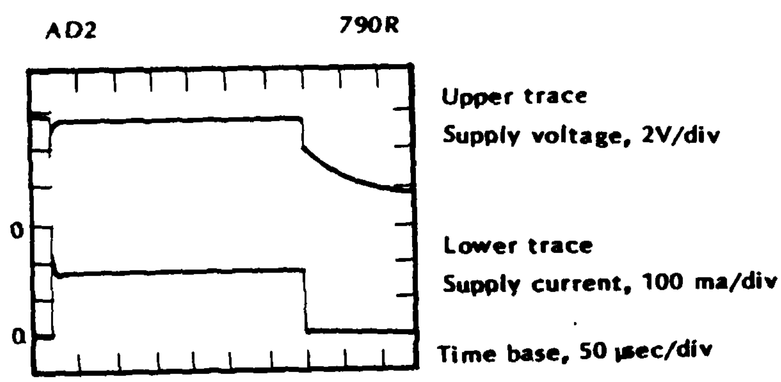
4.5 BIPOLAR DATA

Figures 16a and 16b are oscillograph tracings of the typical latchup response for the 54LS138. The figure shows latchup at two different pulsewidths. During the course of the testing, it was necessary to 're-tune' the Linac in order to attain higher dose and dose rate intensities. As a result, the pulsewidth was wider after 're-tune' (~110 ns).

Table 6 summarizes the latchup results for the bipolar devices tested in this program. No definite indication of a latchup window was found; however, one anomalous result was observed. This anomaly is discussed later.



a. $\gamma \sim 4.2 \times 10^9$, PW ~70 ms, $I_L \sim 160$ ma



b. $\gamma \sim 7.2 \times 10^9$, PW ~110 ms, $I_L \sim 160$ ma

RE-05330

Figure 16. Latchup response of 54LS138, decoder, V_{CC} = 5.5 V (54LS138 - AD2)

Table 6. Summary of latchup window tests for bipolar devices

Device	Date code	Serial	V_{CC} Volts	Window	Dose rate range for latchup R(Si)/sec x 10^{-9}	latchup Current
54LS138	7917	AD1	5.5	NO	3.1 - 3.2	120 mA
54LS138	7917	AD2	5.5	?	3 - 3.03	160 mA
54LS138	7917	AD3	5.5	NO	3.4 - 3.6	160 mA
54LS138	7917	AD4	5.5	NO	--	--
54LS138	7917	AD5	5.5	NO	4.1 - 4.2	150 mA
AD580S	8016	A1	5	NO	--	--
AD580S	8016	A2	5	NO	--	--

5. SUMMARY

5.1 GENERAL RESULTS

All CMOS device types tested exhibited latchup windows; however, there were some unusual results observed. These were: 1) multiple windows, 2) non-repeatable windows and, 3) window creation.

Although one of the two bipolar devices tested did undergo latchup, no conclusive evidence of a window was found. However, there was a single anomaly in the data for one of the bipolar devices.

5.1.1 Multiple Windows

At least one of the CMOS devices in the test had *multiple windows*. That is, at least two regions of latchup were bracketed by regions of no latchup. These data are shown pictorially in Figure 17. How common this phenomenon may be is not known, since the experimental design searched for the existence of a latchup window and was not designed to look for multiple windows. Only in a few cases was the test continued after a single window was found and verified.

The existence of multiple windows is probably not an important observation. It may be an interesting phenomenon, and may help in the explanation of the mechanisms involved; however, the fact that latchup windows exist at all is of greater consequence.

5.1.2 Non-repeatable Windows

In a few cases some difficulty was encountered in characterizing the latchup window. Several pulses of the Linac at the same target dose did not always result in latchup. The explanation of this anomaly may be that the device would have a latchup window extremely narrow in dose rate. One can see from Figure 17 that a latchup window can be extremely small. T' ·fore, slight variations in Linac pulse geometry may put the test outside of the latchup window range.

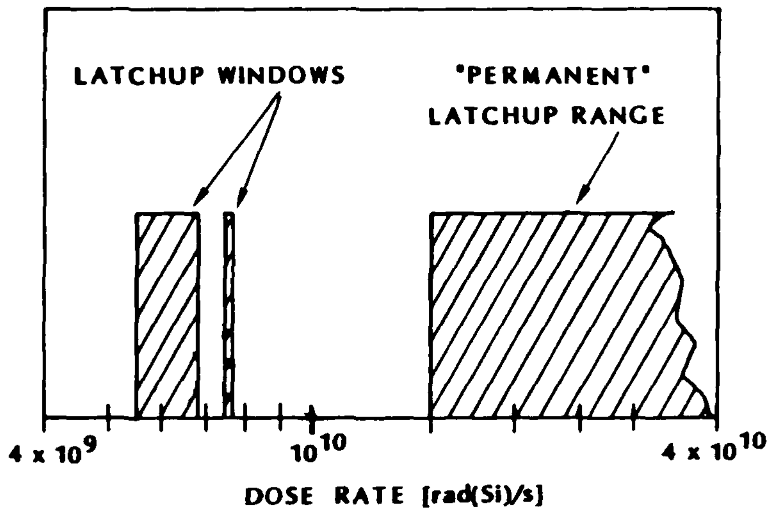
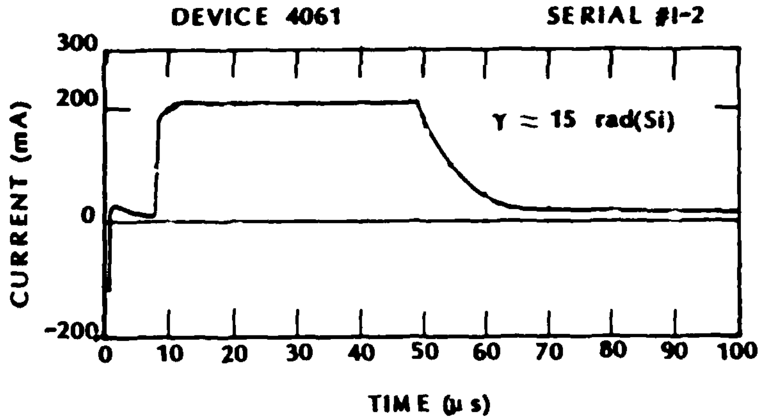


Figure 17. Latchup behavior for the CD4061-CMOS RAM, $V_{DD} \approx 10$ V

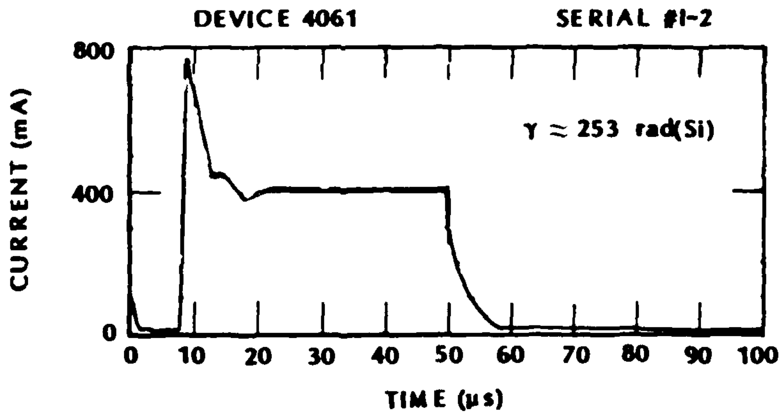
5.1.3 Window Creation

On some devices, two latchup regions were found. One region was the latchup window range itself; the other was a 'permanent' latchup which extended beyond the highest dose rate that could be produced during the test. The latch at the higher dose rate range, in general, had 2 to 3 times larger 'on' current than the current within the window range. Figure 18 is an example of this kind of behavior. At present, it is not known whether all devices which have a latchup window will also permanently latch at a higher dose rate. If all devices which have a window do permanently latch at a higher rate, then a possible method of test may be generated. Future tests should be performed to confirm the two regions of latchup for all devices.

Figure 18 displays tracings of the power supply current for a device tested in both latchup ranges. Figure 18a is the typical response within the latchup window range,



(a) Response in latchup window range



(b) Response in permanent latchup range

Figure 18. Multiple window ranges for CD4094, device no. I-2

while Figure 18b is the 'permanent' latchup response. The fact that the on currents are different (~ 200 mA in the window range; ~ 400 mA for the permanent latch) may indicate that different paths are involved for the two latchup regimes.

On some devices, it was possible to create a latchup window. In at least three cases, a latchup window was uncovered by lowering the applied bias to the test device. When the bias was reduced, the dose rate threshold for the permanent latchup range increased. On the other hand, the dose rate thresholds for the latchup window seemed to be relatively less sensitive to the applied bias. At a higher applied voltage, the permanent latchup threshold may have been lower in dose rate than the latchup window threshold, thus masking the window. At a reduced applied voltage, the permanent latchup threshold would increase to a dose rate level much higher than the latchup window range, thus uncovering the window.

5.1.4 Bipolar Anomaly

In reducing the data on the 54LS138 bipolar device, another anomalous result was detected. The data for this device are displayed in Table 7, arranged in the order of ascending dose rate. Note that at a dose rate of 4×10^9 rad(Si)/s, a latchup was not obtained.

The result was not repeated, and therefore, the single anomalous result cannot be offered as conclusive evidence of a latchup window in bipolar devices. The instability of the Linac beam made repeated tests at a single dose point impractical at the facility used.

5.1.5 Temperature Sensitivity

Although no direct measurement of the temperature sensitivity of latchup and latchup windows was made, a sensitivity to ambient temperature was noted. Early in the tests it was noted that as the ambient temperature in the test cell was lower, extreme difficult was encountered in reproducing results previously attained. The test cell temperature varied at least 3°C from the beginning of a test day to the end of a test day. Some of the temperature sensitivity in the CMOS tests was compensated for by slightly raising the applied voltage (approximately 0.1 to 0.2 volts).

The temperature sensitivity of latchup and latchup windows is an important and interesting problem. No methods of temperature control were designed into the tests

Table 7. Latchup data summary, 54LS138, #AD2

Dose [rad(Si)]	PW (nsec)	Dose Rate [rad(Si)/sec]	Latchup
136	70	1.94×10^9	no
240	110	2.18×10^9	no
280	110	2.55×10^9	no
188	70	2.69×10^9	no
330	110	3.0×10^9	no
212	70	3.03×10^9	yes
380	110	3.45×10^9	yes
255	110	3.64×10^9	yes
259	70	3.7×10^9	yes
440	110	4×10^9	no
294	70	4.2×10^9	yes
295	70	4.21×10^9	yes
296	70	4.23×10^9	yes
300	70	4.29×10^9	yes
302	70	4.31×10^9	yes
670	110	6.09×10^9	yes
790	110	7.18×10^9	yes

reported here. However, the extreme sensitivity noted here indicate that future latchup tests should pay careful attention to temperature sensitivities.

5.2 CONCLUSIONS

This program tested 3 CMOS device types for latchup windows. These windows were found and documented. Data were taken that clearly demonstrated the existence of the windows by displaying the dose rate range over which latchup occurred. At the present time, no explanation of the latchup window phenomenon is offered; however, future work will be initiated to investigate the physics of this phenomenon.

A limited number of two types of bipolar devices were tested under this program. Although no conclusive evidence of latchup windows was found, a single anomalous result did occur.

Future work in this area should include mechanism studies performed on devices which have demonstrated latchup window behavior. In addition, further tests of bipolar devices should be made.

APPENDIX A

LATCHUP WINDOW TEST PLAN (CMOS)

A1. INTRODUCTION

A1.1 PURPOSE

This document presents the general methods and procedures to accomplish the objectives of the latchup window program being conducted at JAYCOR. The document describes the test method, devices, and facility to be used in the tests.

A1.2 OBJECTIVE

The objective of this program is to investigate the phenomenon of latchup windows. The specific test objectives are threefold.

1. To obtain conclusive evidence for the existence of latchup windows.
2. To find specific devices which exhibit latchup windows for use in future study programs.
3. To test for the existence of latchup windows in bipolar devices.

A1.3 SCOPE

The scope of these tests is limited to linear accelerator tests and devices. The Linac to be used will be the White Sands Linear Accelerator. The principal technologies to be tested will be CMOS devices, with bipolar devices being used as they become available.

A1.4 SEMICONDUCTOR PARTS

The devices available to be used in this program are shown in Table A1. The device type and source are shown in the table.

Other devices will be included in the program as they become available. Some candidate devices which we are trying to obtain are:

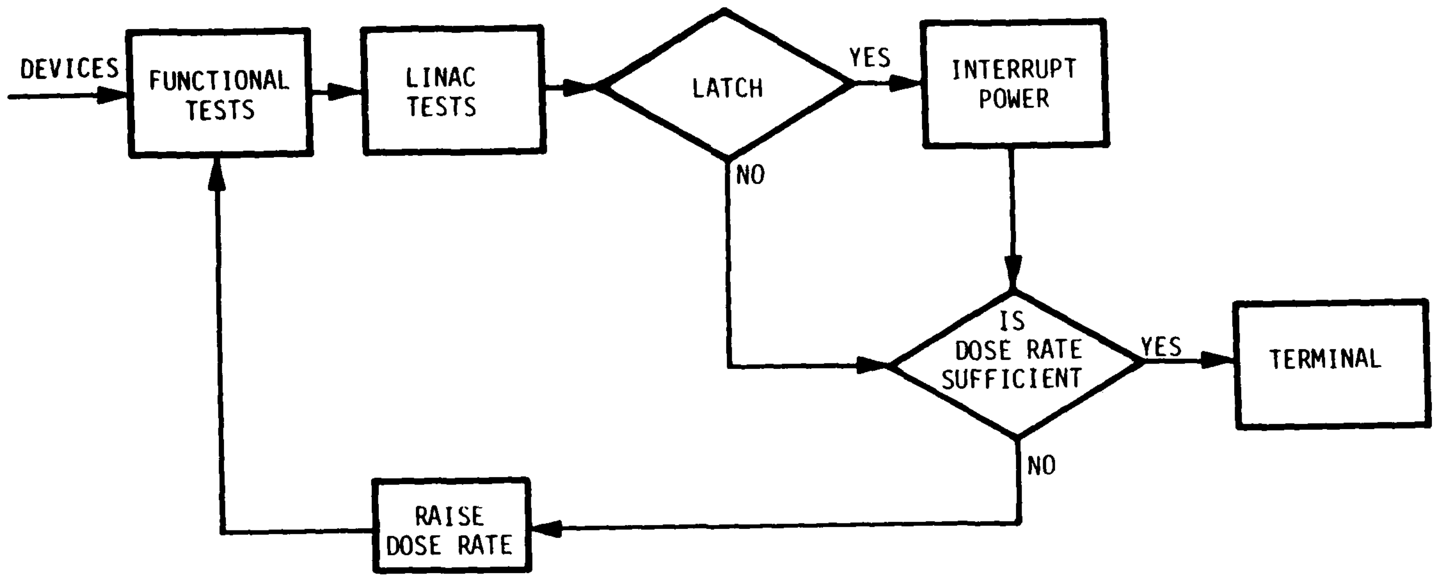
1. 54LS124
2. AD581U
3. CD4508
4. TRIDENT 244 RAM

Table A1. CMOS devices on hand for latchup window program

Device type	Number	Source	Remarks
CD4047	24	IRT	Original source was Sandia
CD4047	19	IRT	Commercial purchase
CD4047	20	JAYCOR	Commercial purchase
CD4047	20	CRANE	Commercial purchase
CD4061	24	IRT	Original source was Sandia
CD4061	5	SANDIA	-
CD4061	20	JAYCOR	Commercial purchase
CD4094	18	IRT	Original source was Sandia
CD4094	9	IRT	Commercial purchase
CD4094	21	IRT	Commercial purchase
CD4094	20	JAYCOR	Commercial purchase
CD4094	5	SANDIA	-
CD4094	20	CRANE	Commercial purchase

A1.5 TEST FLOW

Figure A1 shows the test flow diagram for the Linac tests. Notice that functional tests will be performed after each Linac pulse to determine if the device has been damaged. A power removal circuit has been incorporated to remove power to bring the device out of latchup. The power removal circuit is actuated by sensing the magnitude of the current that the device is drawing. More will be said about this circuitry later.



RE-04475

Figure A1. Test flow diagram for latchup window program

A2. EQUIPMENT

A2.1 FACILITY

The tests covered by this test plan will be performed at the White Sands Linear Accelerator Test Facility. The accelerator is operated by the Nuclear Weapons Effects Division of the Army Missile Test and Evaluation Directorate. The Linac is a two-section, S-band accelerator which operates in the range of 1-43 MeV. Pulsewidths can be varied from 0.03 to 10 μs.

A2.1.1 Operating Characteristics

The operating characteristics of the White Sands Linac are summarized in Reference A1. Some of the more pertinent features as they relate to those tests are reproduced below for completeness.

A2.1.2 Beam Geometry

Figure A1 shows the angular beam divergence as a function of energy. These tests will be performed for beam energies in the range of 15-20 MeV which results in a high degree of collimation. Isodose contours are shown in Figure A2, again showing the degree of collimation in the beam. It will probably be necessary to use a scatterer to spread the beam in order to assure uniform dose across the test devices.

A2.1.3 Beam Intensity

Figure A3 shows the electron flux distribution profile for several distances from the output window. Coupling this with Figures A4 and A5 gives us an estimate of the relative beam intensity. Figure A4 shows the relative intensity as a function of distance, while Figure A5 gives the radiation in intensity with beam current.

A1. Experimenters' Guide for the Nuclear Weapons Effects Laboratory at White Sands Missile Range, New Mexico.

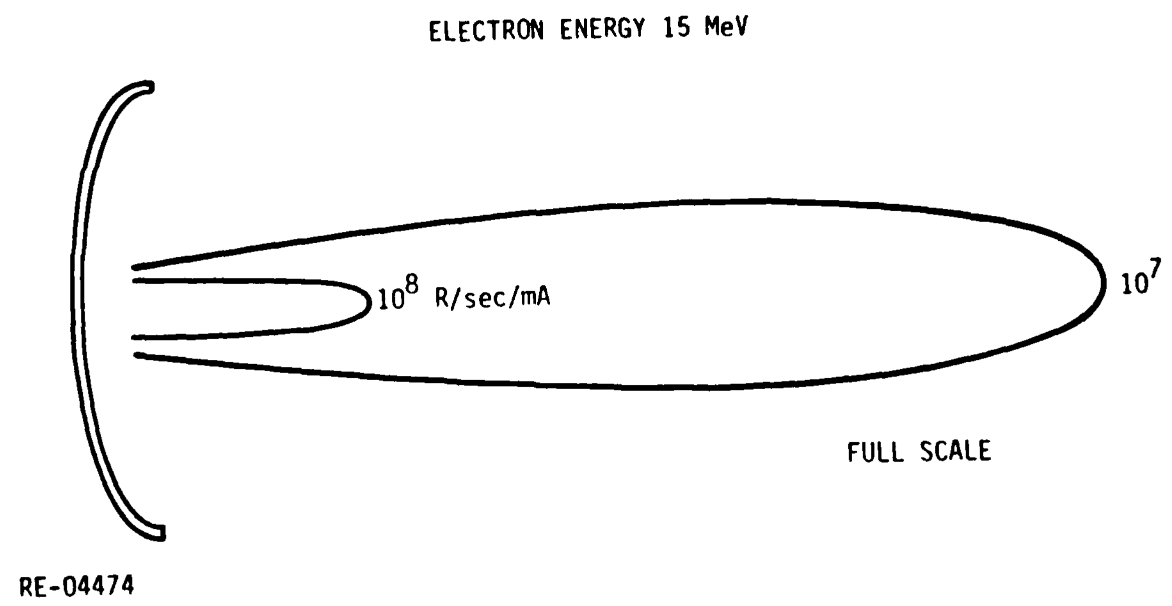
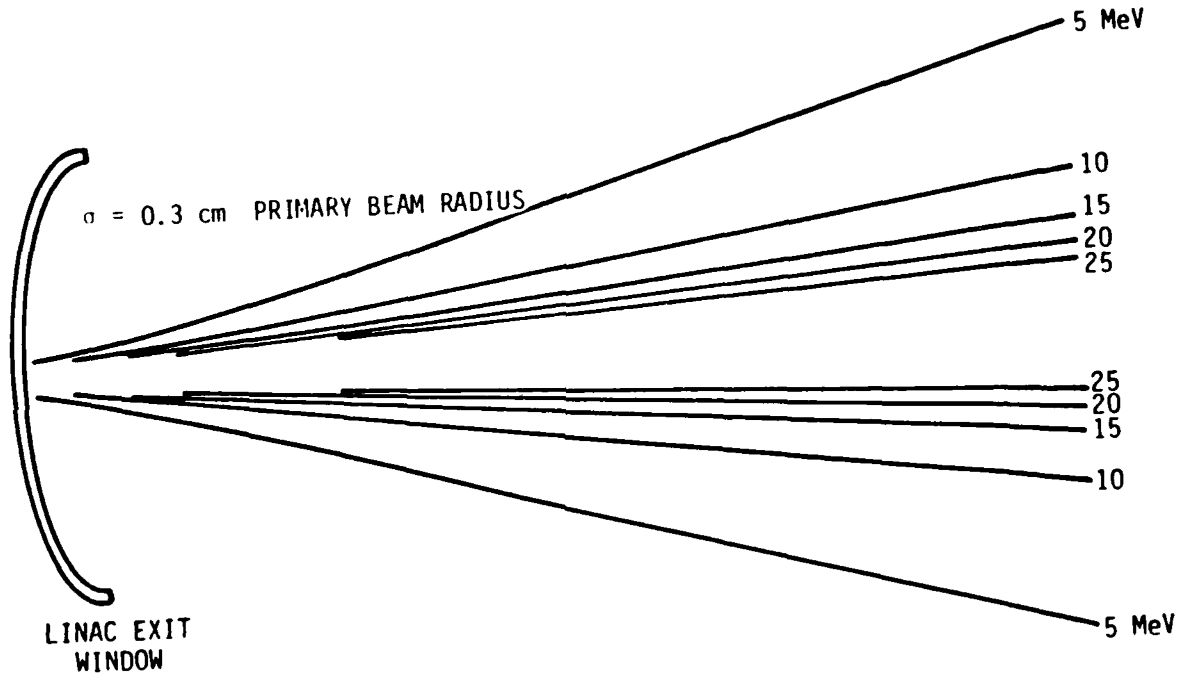
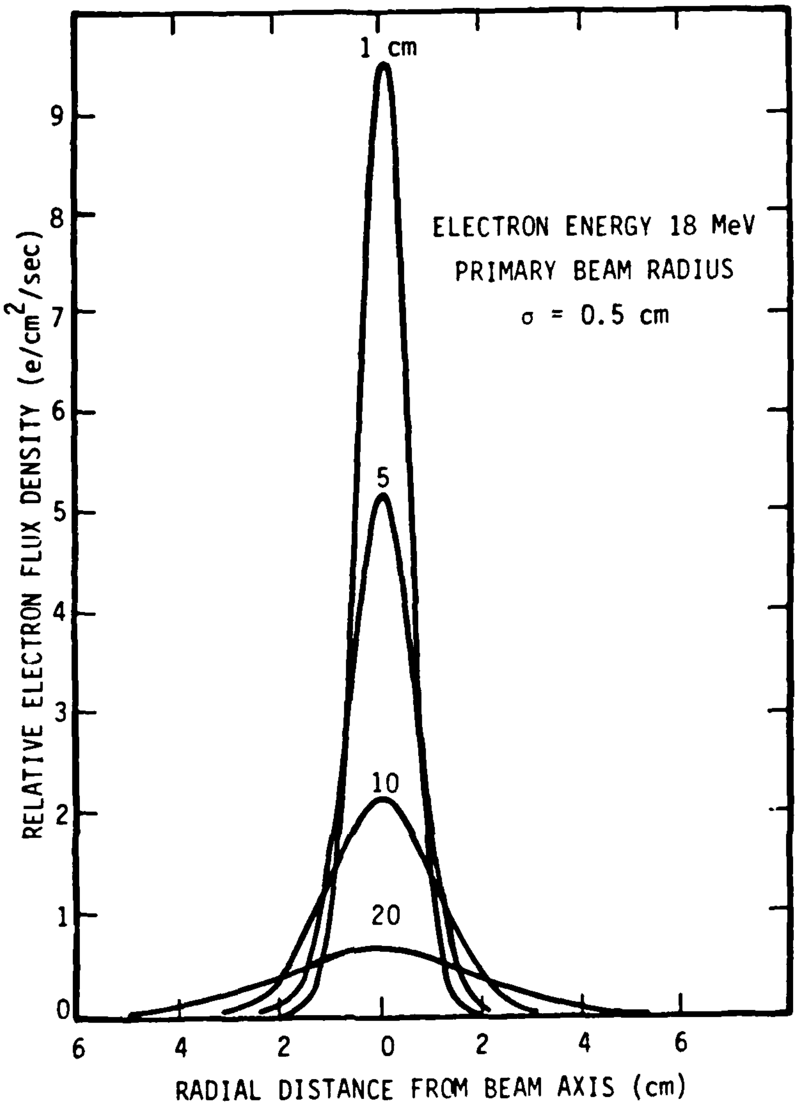


Figure A2. Isodose contours for a 15 MeV beam issuing from the Linac window (Ref. 1)



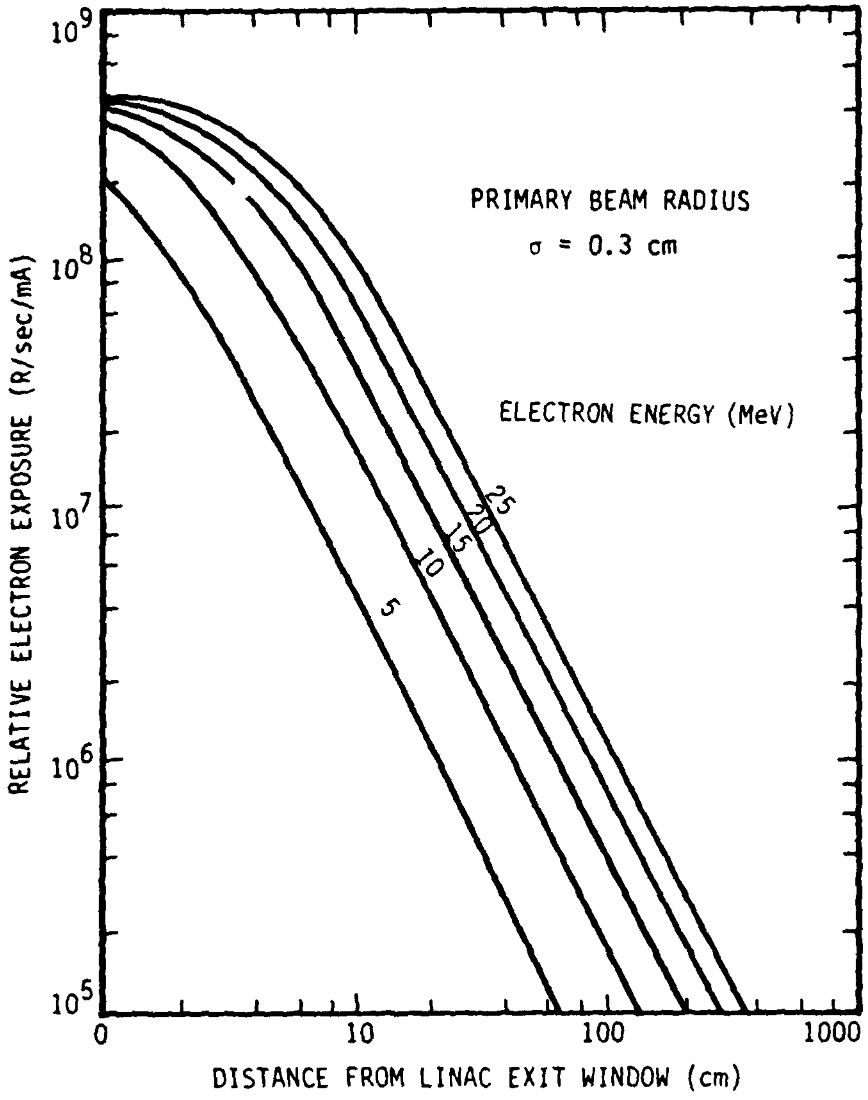
RE-04473

Figure A3. Angular divergence of electrons caused by scattering at the Linac exit window (Ref. 1)



RE-04472

Figure A4. **Profiles of electron distribution across the beam at increasing distances from the output window (Primary beam was 1 cm in diameter) (Ref. 1)**



RE-04471

Figure A5. Electron exposure rates for various energies at increasing distances from the exit window (Ref. 1)

It is clear that an acceptable dose rate range can be achieved at reasonable distances from the Linac window. It appears that practical exposure distances will be in the range of 10 to 100 cm.

A2.1.4 Spectrum

Another characteristic of importance for these tests is the machine electron energy spectrum. A typical energy spread is shown in Figure A6. About 90% of the electrons are within 2.5 MeV of the mean energy.

A2.1.5 Scattering

To assure uniform exposure to the entire device cross section, an electron scatterer will be used. This will reduce the problem of 'hot spots' and make axial alignment less critical. Figure A7 shows a plot of electron scattering angles as a function of aluminum scattering thickness. A 1/8-inch aluminum scatter is expected to be used in these tests.

A2.2 EQUIPMENT

The White Sands Linac Facility is equipped with a significant amount of support equipment. This equipment includes power supplies, oscilloscopes, tape recorders and transient digitizers. In terms of support equipment, these tests will require:

Techtronix 7912 transient digitizers
Power supplies
Digital voltmeter
Movable table for Linac exposure
Dosimetry (TLDs) and reader.

In addition, equipment supplied by JAYCOR will include:

HP Computer/controller
JAYCOR 7600 switch matrix
Test fixtures
Cables
PIN diode
Bias circuitry.

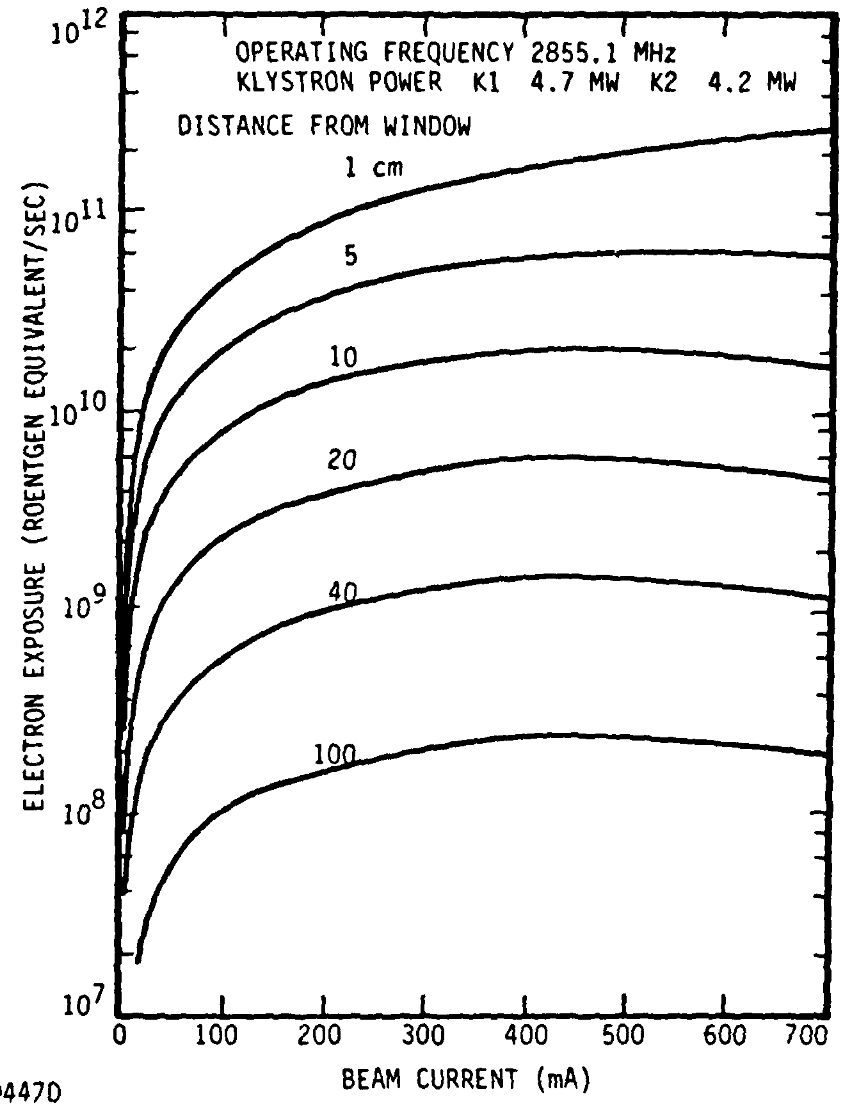
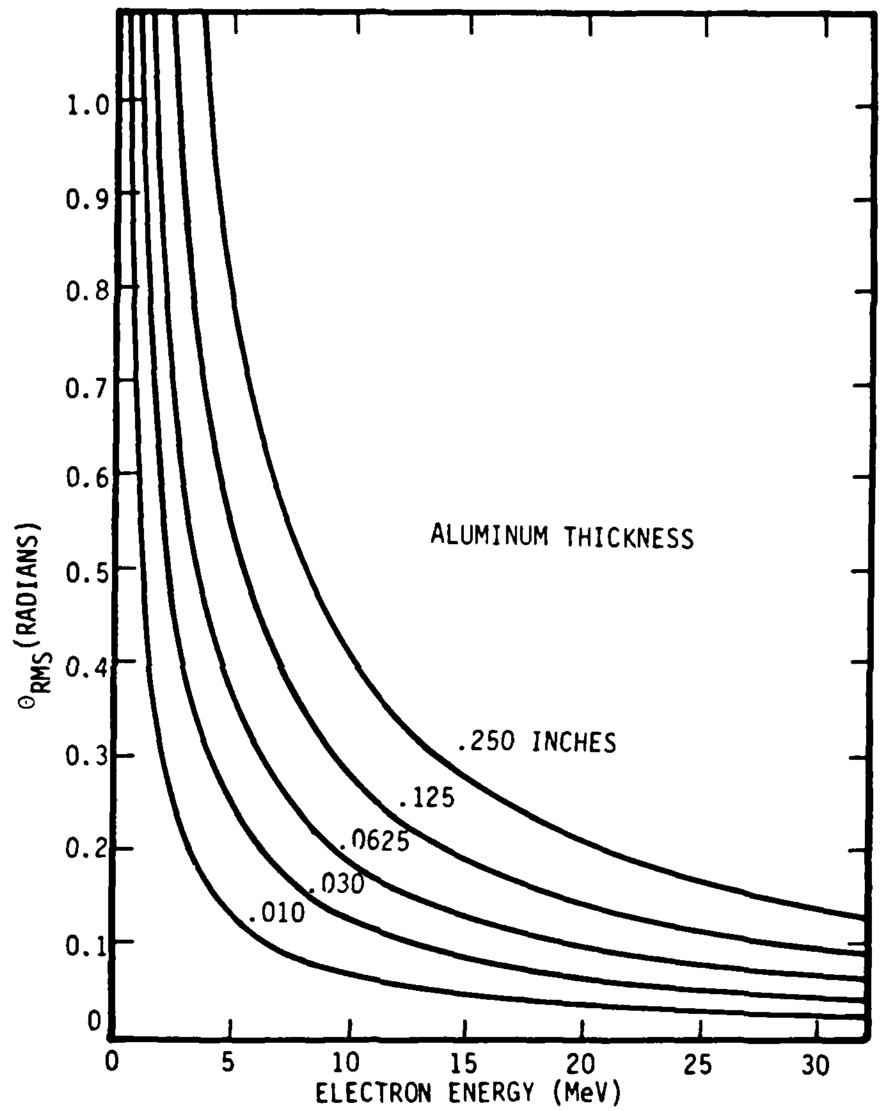
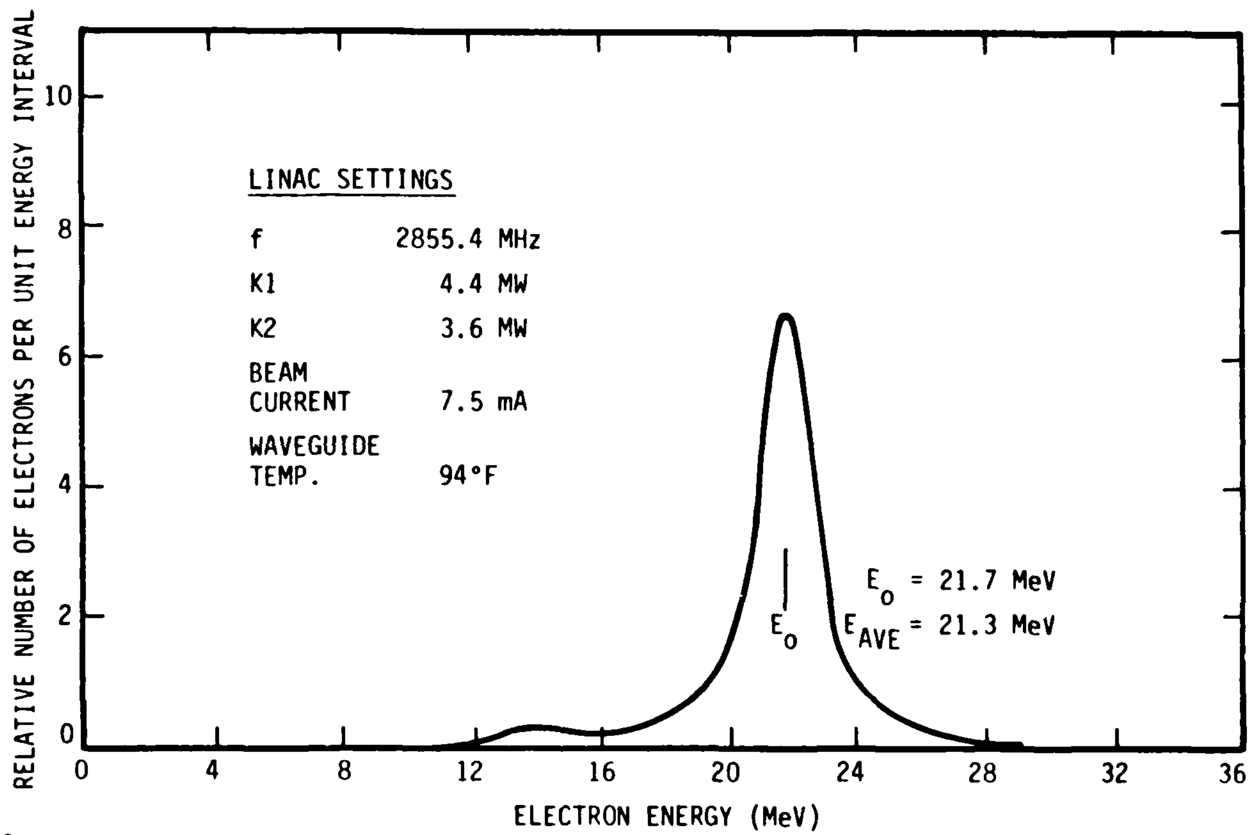


Figure A6. Electron exposure rates for increasing beam current at various distances (Ref. 1)



RE-04469

Figure A7. **Scattering angle for electrons striking an aluminum sheet (from Bethe and Ashkin, Exp. Nucl. Phys., Segre (ed.), Wiley, 1953, p. 285)**



RE-04468

Figure A8. Electron energy spectrum for WSMB Linac (Ref. 1)

A3. GENERAL REQUIREMENTS

The general testing, handling and data-recording requirements for parts used in this test program are described in this section.

A3.1 PARTS CONTROL

Upon receipt, all parts to be tested will be serialized. A parts log will be maintained and will contain records of all testing and the radiation levels each device receives.

A3.2 ELECTRICAL TESTS

All CMOS devices will be functionally tested before each radiation exposure. This will be accomplished by use of the JAYCOR-designed circuitry. The HP-85 will automatically functionally test the devices before each subsequent radiation exposure.

Latchup in these circuits will be detected by observing an increase in power supply current to the devices. An increase in current will trigger a shutdown circuit in order to prevent damage to the device.

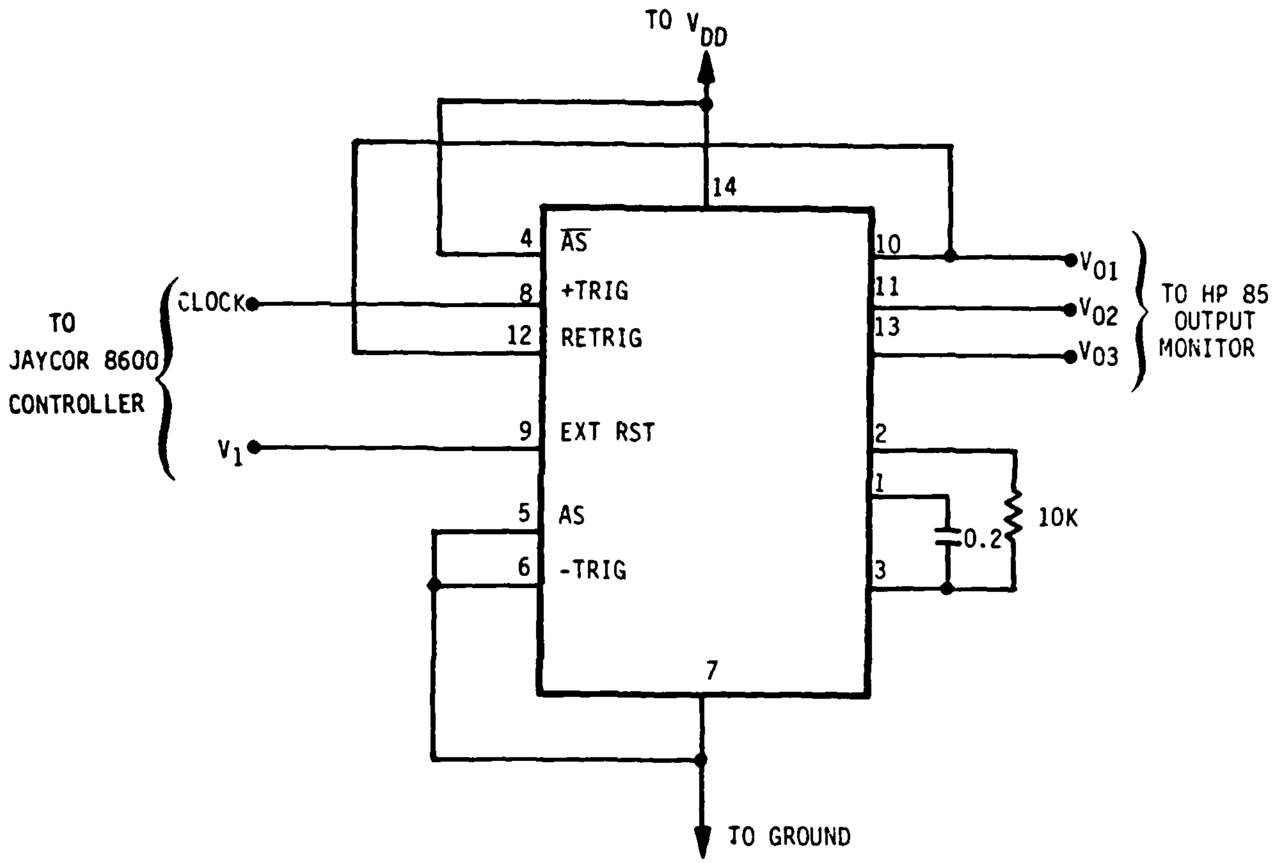
A3.3 DEVICE CIRCUITRY

Figures A9, A10, and A11 show the circuitry to be used for testing the CMOS devices. These circuits are adapted from the circuitry used by IRT Corporation when the latchup window phenomenon was first observed. Modifications have been made to accommodate the JAYCOR test circuits and to make the test fixture portable.

A3.4 TEST CIRCUITRY

A block diagram of the JAYCOR test circuitry is shown in Figure A12. This circuit consists of:

1. A threshold detector
2. A control switch and power reset circuit
3. Device interface circuitry



RE-04466

Figure A9. Electrical test conditions for latchup tests of the CD4047 A

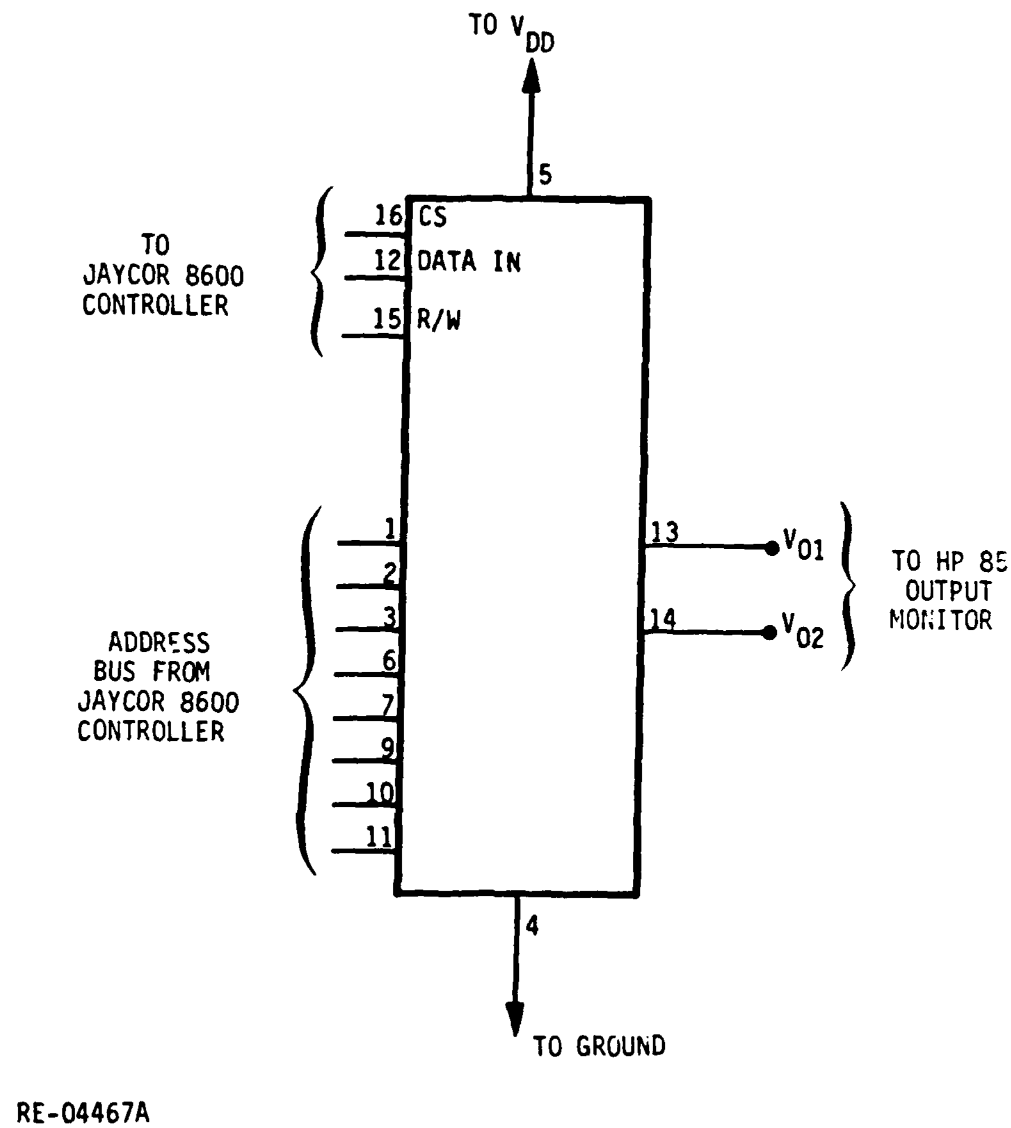


Figure A10. Electrical test conditions for latchup tests of the CD4061A

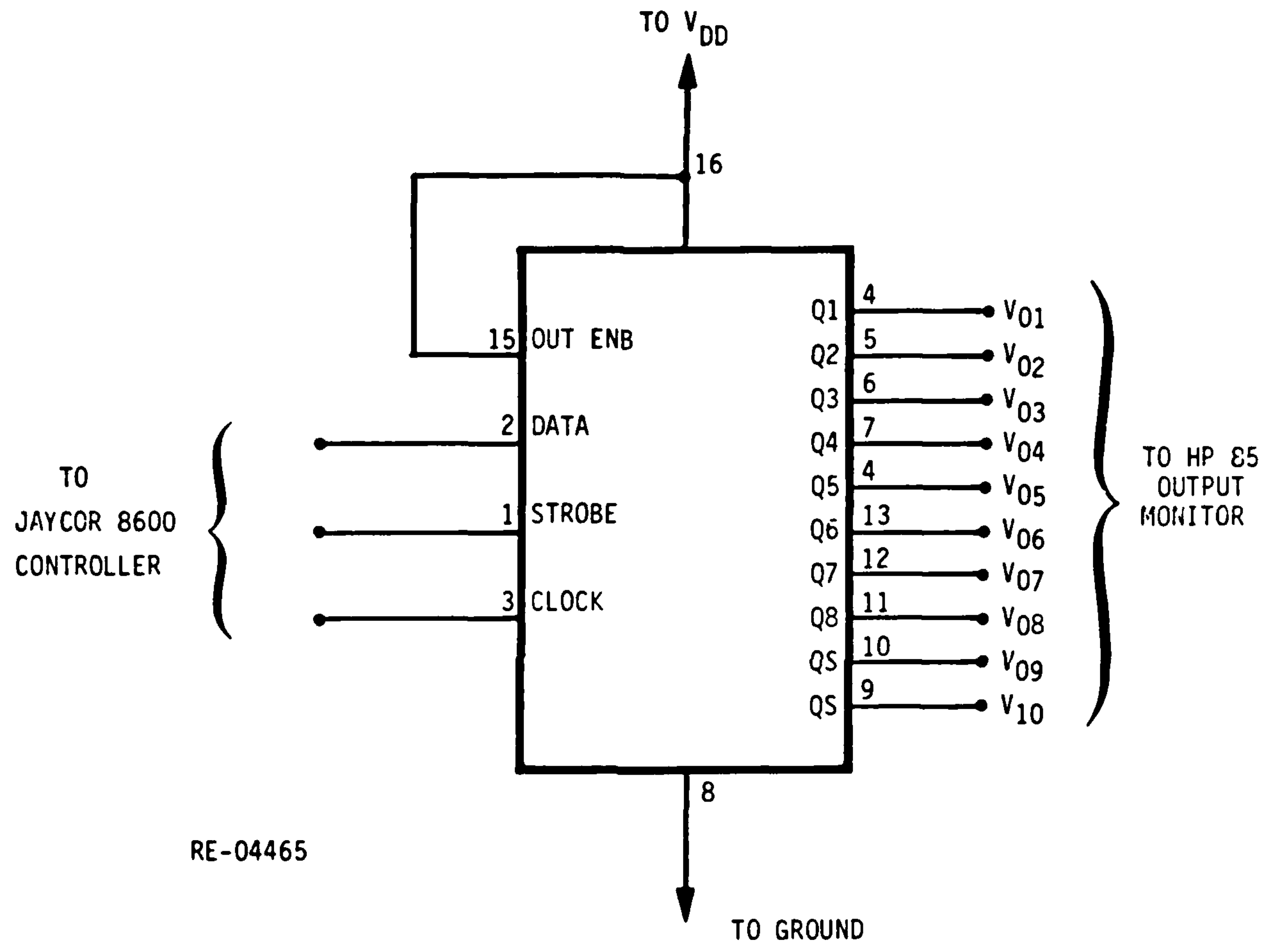


Figure A11. Electrical test conditions for latchup tests of the CD4094A

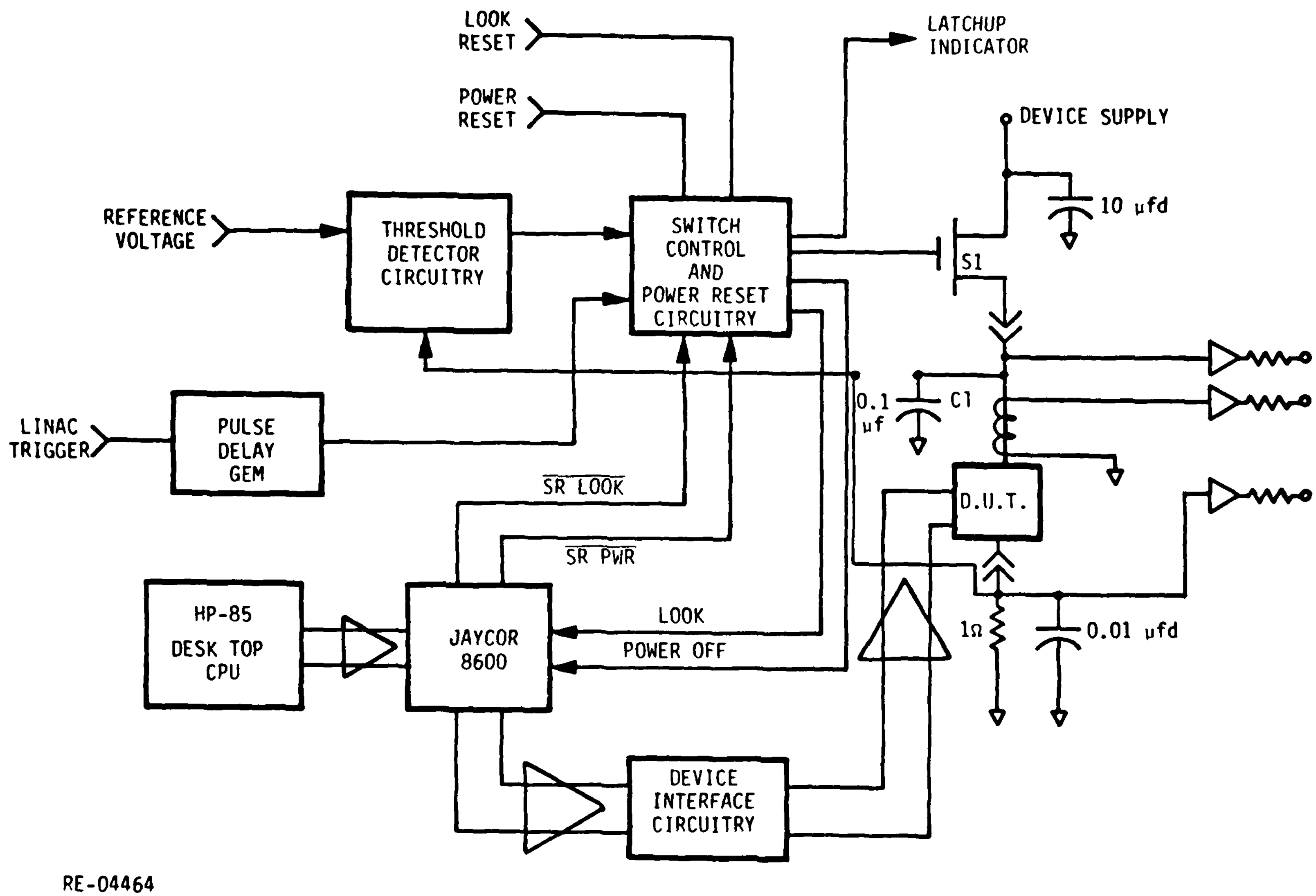


Figure A12. Test circuit block diagram

4. Control circuitry
5. Monitor circuitry.

A3.4.1 Threshold Detector

The threshold detector senses the magnitude of the device-under-test power supply current. At a set time, variable from 1 μ s to 500 μ s, the circuit determines if the current is greater than a predetermined threshold current. If the current is greater than the threshold, the circuit removes power from the device.

A3.4.2 Control Switch and Power Reset Circuitry

If the power supply current is greater than the threshold, power is removed by turning off the VMOS switch S1. The time constant for removing power is determined by the capacitor C1, and the magnitude of the latchup current. This time constant is given approximately by:

$$T \approx \frac{1 \times 10^{-6}}{I}$$

A3.4.3 Device Interface Circuitry

The device interface circuitry provides the biases and control signals to properly bias the device for latchup and to exercise the device after the test. Separate 'personality' circuits are constructed for each device type.

A3.4.4 Control Circuitry

The control circuitry consists of an HP-85 desktop computer, which interfaces to the device through a JAYCOR 8600 IEEE bus control/interface unit. This system provides the control to set, reset, and exercise the device for each test.

A3.4.5 Monitor Circuitry

The power supply current is monitored using a 1-Ω resistor to sense the current. The 1-Ω resistor is bypassed for transients during the ionization pulse. Thus, the resistor monitor measures the latchup current should the device latch up.

A CT1 current transformer is used to monitor the fast transients during the pulse. In this way, both the fast transients and the steady-state current are able to be monitored.

In addition, the supply voltage at the device power supply input terminal is monitored. In this way, any sag in the supply voltage can be easily detected.

A3.5 TEST FIXTURE

The test fixture consists of an aluminum/lead shield plate with an aluminum structure for mounting the circuitry. A schematic drawing of the fixture is shown in Figure A13. This fixture was designed by the Naval Weapons Support Center and has been used at the White Sands Linac facility. JAYCOR has adapted the fixture for the latchup window tests.

A3.6 DOSIMETRY

Calibration of the dose-rate vs. distance characteristics will be done using thermoluminescent dosimeters. Pulse shape and shot-to-shot variability will be done using a PIN diode. The PIN diode response will be recorded for each pulse of the Linac.

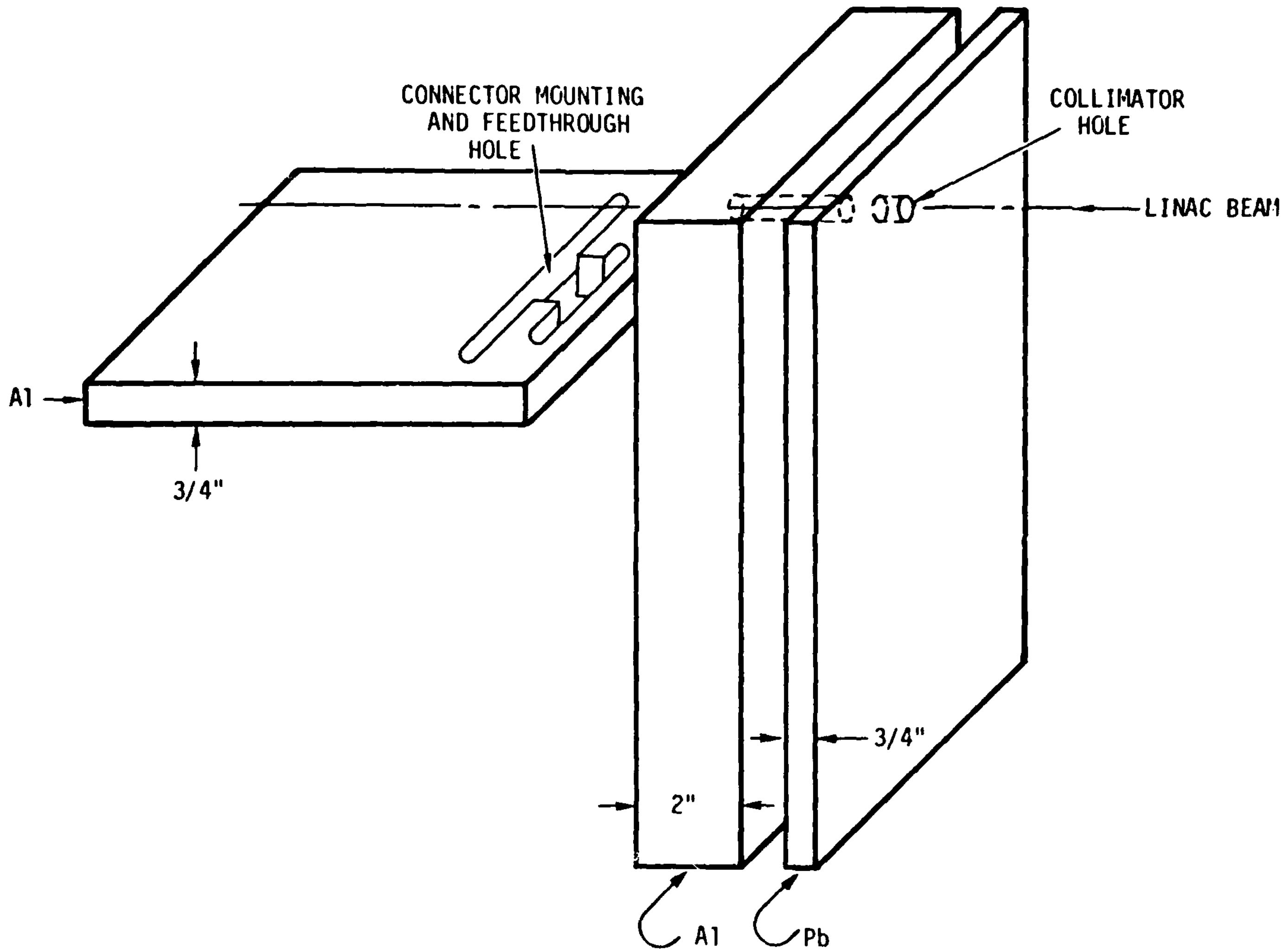


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Figure A13. Mechanical test fixture

A4. TEST SEQUENCE

A4.1 TEST DEVICES

In general, the order of tests will be as follows:

1. Devices which have shown a latchup window previously.
2. Devices of the same type and lot which have not yet been tested.
3. Devices of the same type which have not shown a latchup window but have latched.
4. Devices of commercial quality which have not yet been tested.

This sequence is summarized in Table A2.

A4.2 TARGET RADIATION

The pulsewidth to be used is approximately 65 ns. The target dose levels to be used are summarized in Table A3. These values are based on the expected latchup thresholds as previously measured for these devices, the first level being about an order of magnitude lower than the previously measured level. The dose (and the corresponding dose rate) is increased by about one-half an order of magnitude up to the point of latchup threshold, then increased by smaller steps to search for the window.

A4.3 DATA

The following information is to be recorded for each test sequence:

1. Date of test
2. Equipment list
3. Experimenters
4. Temperature
5. Power supply settings
6. Calibration information
   a) Scopes
   b) Movable table
   c) Dosimetry

Table A2. Test devices

Sequence	Device type	Serial number	Source
1	CD4061	5-6,11,23	IRT/Sandia
2	CD4094	S-24-	IRT/Sandia
		P-1,2,3,4,5,9	IRT/Commercial
3	CD4061	111,112,113,114,115	Crane/Sandia
4	CD4094	1,2,3,4,5	Crane/Sandia
5	CD4061	S-1,2,4,5,7-10,12-23	IRT/Sandia
6	CD4094	S-1,2,4-9,11-15,17,20,22	IRT/Sandia
	CD4094	P-6,7,8	IRT/Commercial
7	CD4061	J-1-20	JAYCOR/Commercial
8	CD4094	J-1-20	JAYCOR/Commercial
9	CD4094	J-1-20	JAYCOR/Commercial
10	CD4047	S-1-25	IRT/Sandia
11	CD4094	1-20	Crane/Commercial
12	Others		

Table A3. Approximate target dose values by device type

rads (Si)		
CD4061	CD4094	CD4047
1	10	10
5	50	50
10	100	100
20	200	200
40	400	400
60	600	600
100	800	800
500	1000	1000
1000	2000	2000
2000		

Note: These dose levels are target values. The condition of the test will determine exact levels used.

7. Linac energy

8. Linac target pulse

The following information is to be recorded for each Linac pulse:

1. Device number and identification

2. Dose level

3. Pulsewidth

4. Latchup/no latchup

5. Latchup current

6. Functionality

The following data are to be recorded on the Tektronics 7912 transient digitizers:

1. PIN diode response

2. Device voltage

3. Device transient current

4. Device steady-state current.

APPENDIX B

LATCHUP WINDOW TESTS

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ABSTRACT

This paper presents the results of a test program designed to investigate the latchup window phenomenon. Data on three CD4000 type CMOS were taken to clearly demonstrate the existence of windows and to document the dose rate range where latchup occurred. The paper also describes some anomalous results which were encountered in the tests.

INTRODUCTION

This paper addresses the very important issue of latchup windows in integrated circuits. This is a serious problem and requires careful consideration in each individual case of system design. Latchup may cause system failure through burnout of the device or through an upset of the circuit in which latchup occurs.

The existence of a latchup window was first reported by researchers performing latchup testing of MOS integrated circuits.[1,2] It was found that latchup would occur in some devices for only a small range of dose rates. At dose rates below a critical value, the device would not experience latchup. A second, higher dose rate was found above which latchup again did not occur.

The purpose of the tests performed in this program was to demonstrate that latchup windows do in fact exist. Although the previous studies of latchup windows[1,2] discovered a number of CMOS devices which apparently had latchup windows some uncertainties still exist in the minds of many designers. Therefore, the first objective of the tests was to provide a clear demonstration of the existence of the latchup window phenomenon. The tests were limited to CMOS devices of the type which had previously been reported to have latchup windows. These were the CD4047, CD4061, and the CD4094 CMOS integrated circuits.

TEST PROCEDURE

The latchup window tests were performed at the White Sands Linear Accelerator (Linac) Test Facility.[3] The accelerator is operated by the Nuclear Weapons Effects Division of the Army Missile Test and Evaluation Directorate. The Linac is a two-section, S-band accelerator which operates in the range of 1-43 MeV. A nominal 70 ns pulsewidth was used for these tests, with beam energy of ~20 MeV.

A variety of measuring and support equipment was provided by the White Sands Test Facility. All radiation response data were recorded on Tektronix 7912 transient digitizers. Four channels of data were recorded for each pulse of the Linac.

Dosimetry was performed using a PIN diode mounted near the test device package. The PIN was periodically calibrated against the thermoluminescent dosimetry (LD), provided by the White Sands Facility, and the calibration was made over the full range of expected dose.

Figure 1 is a plot of the dosimetry performed at the White Sands Facility. One can see the expected saturation of the PIN at higher dose rates. It is important to note that the maximum dose available was ~2800 rad(Si). The minimum dose used was ~5 rad(Si). Thus, the dose rate range used for these tests extended from ~10^8 rad(Si)/s to ~4×10^{10} rad(Si)/s.

A block diagram of the test circuitry used for these tests is shown in Figure 2. This test circuit consists of several parts: (1) a threshold detector, (2) a control switch and power reset circuit, (3) monitor circuitry, (4) interface circuitry, and (5) control circuitry.

The threshold detector senses the magnitude of the device-under-test (DUT) power supply current. At a preset and variable delay time, the power supply current is sensed, and

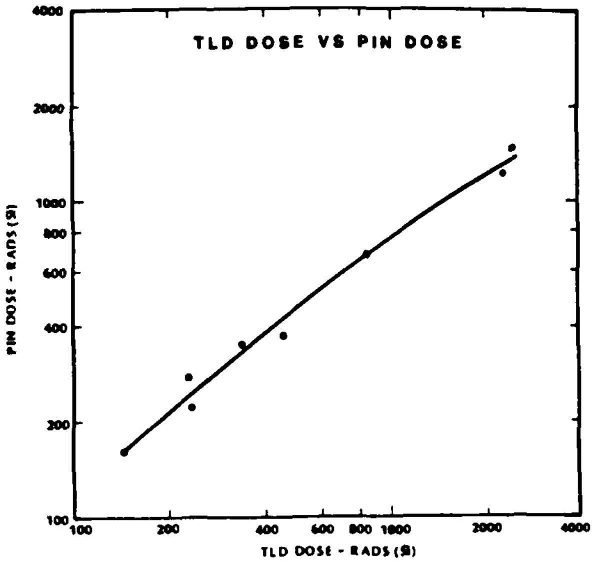


Figure 1. PIN diode calibration for latchup tests

should this current be greater than a predetermined threshold current, the circuit initiates power removal from the device via the VMOS switch S1.

The time required for removing power after the delay time is determined by the capacitor C1, a 0.1 μF capacitor, and the magnitude of the latch current. This time is given approximately by:

$$T = \frac{Q_{C1}}{I} = \frac{V_{C1} \times C1}{I} = \frac{10 \times 0.1 \times 10^{-6}}{I} \quad .$$

For a nominal latch current of 200 mA and a supply voltage of 10 V, the power would be removed in ~5 μs.

The power supply current was monitored using a 1-Ω resistor bypassed by a 0.01 μF capacitor. For monitoring fast transients during the ionization pulse, a Tektronix CT1 current transformer was used. In this way, both the fast transients and the steady-state current were monitored.

In addition, the supply voltage at the device power supply input terminal was monitored. Any sag in the supply voltage was easily detected.

The device interface circuitry provides the proper biases and control signals to bias the device for latchup testing and to exercise the device after the test. Separate "personality" circuits were constructed for each device type. These circuits interface each individual device with the bias circuitry and controller.

The control circuitry consists of an HP-85 desktop computer, which interfaces to the device through a JAYCOR 8600 IEEE bus control/interface unit. This system provides the control to set, reset, and exercise the device for each test. All of the devices were functionally tested and set in a predetermined state before each radiation exposure, by use of the circuitry described above and the HP-85 computer.[4]

The testing technique to document latchup windows was to irradiate the device under test with at least one pulse at a dose rate below the threshold, and at least two pulses above the threshold for latchup, but within the window. This demonstrates that the latch condition was repeatable. Then at least two pulses were required above the latchup window range to

*Work sponsored by the Defense Nuclear Agency under Contract No. DNA 001-81-C-0281.

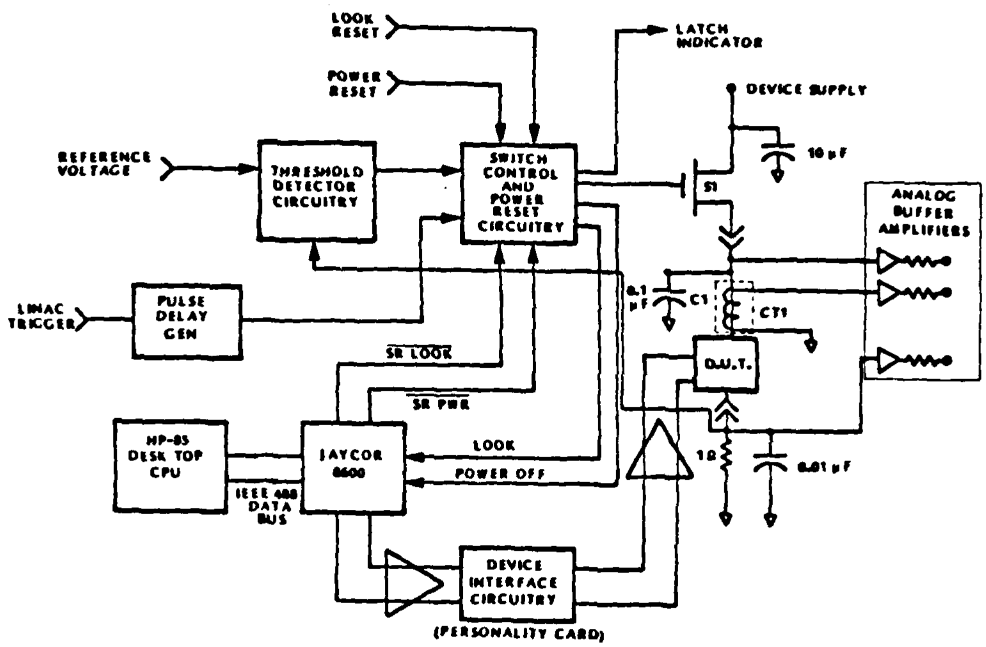


Figure 2. Block diagram of latchup test circuitry

clearly demonstrate no latchup occurred at the higher dose rates. Finally, another pulse was taken within the latchup window range to assure that the window still remained after all the previous testing.

RESULTS

The CMOS devices which were tested in this program are listed in Table 1. All the devices were RCA CD4000-series devices; however the source and pedigree of the devices did change. The table presents the device type, the number tested, and the controlling organization which acquired the devices.

Many of the devices had been tested for latchup windows in a previous program,[1,2] and latchup windows were found in some of those devices. Devices that had never been previously tested are indicated in the table.

The tracings of Figure 3 are typical response curves for the power supply current of the CD4047, device number S-3. The first trace is the response at a dose below the window range. Traces B and C indicate latchup at two different doses within the window range. Finally, trace D is the response at a dose above the window range. The device has not latched at this dose, clearly demonstrating a latchup window.

Table 2 summarizes the results for all the CD4047 devices tested in this program. An important point to be noted is that one device in lot 923 did not have a window at 10-volts applied bias. However, when the bias was slightly reduced, a window was found. Thus, in some cases, the existence of a latchup window seems to have a bias dependency. It may very well be that in this case, the upper bound of the latchup window was beyond our testing capability at the 10-volt bias. Decreasing the bias may have reduced the upper bound of the latchup window to a dose rate within our testing capability.

The graphs of Figure 4 are tracings of a similar latchup window response for the CD4061, device number S-113. These curves demonstrate a window with a magnitude of about 5 rad(Si). It is clear that a narrow window, as indicated here, can easily be missed by ordinary latchup screens, particularly when conducted at FXR facilities which do not exhibit good pulse reproducibility.

Table 3 summarizes the results for all the CD4061 device types tested in this program. Once again, a latchup window was created by lowering the voltage applied to the device.

Type	Number tested	Source	Latchup window	Previous window
CD4047A	3	IRT	1	0
CD4047B	2	JAYCOR	0	0*
CD4047A	3	SANDIA	2	2
CD4061A	5	IRT	5	5
CD4061A	3	JAYCOR	0	0*
CD4061A	4	SANDIA	4	0*
CD4094B	10	IRT	3	7
CD4094B	4	JAYCOR	0	0*
CD4094B	2	CRANE	0	0*
CD4094A	3	SANDIA	2	0*

*not previously tested.

Table 1. Summary of latchup window results

The graphs of Figure 5 are tracings which provide an example of a latchup window for the CD4094, device number P-2. The response is similar to the other devices, but, the threshold for latchup and the dose rate range of the window are both larger.

Device number	Lot	V_{DD} supply volts	Window	Dose range for* latch threshold Ṙ (Si)	Dose range for* no latch threshold Ṙ (Si)
S1	7709	10	yes	132 - 133	133 - 135
S2	7709	10	no	140 - 173	-
S3	7709	10	yes	100 - 144	149 - 150
I1	927	10	no	124	-
I2	927	10	no	61 - 69	-
C10	923	10	no	206 - 217	-
		9.5	yes	257 - 270	611 - 670
C22	923	10	no	212 - 268	-
C24	923	10	no	139 - 271	

*The two values for each threshold indicate the range in which the threshold occurs.

Table 2. Summary of latchup window results for CD4047 devices (P.W. ≃ 70 ns)

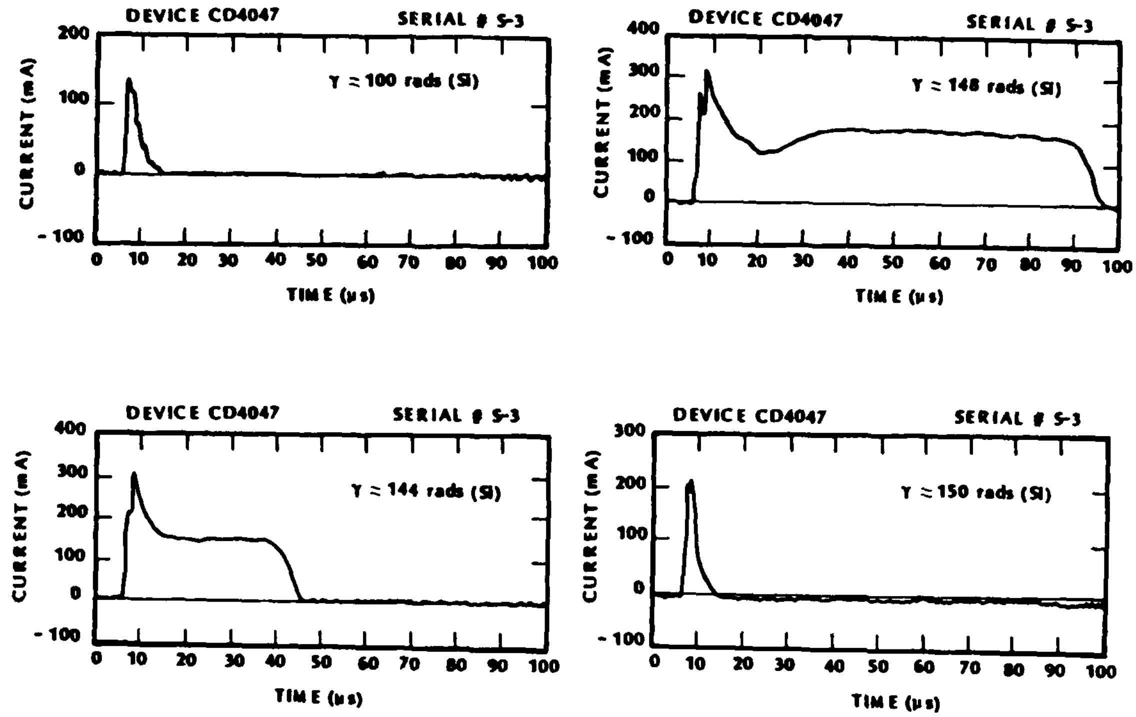


Figure 3. Latchup window behavior for the CD4047-CMOS multivibrator, $V_{DD} \approx 10$ volts (CD4047A, Lot 7709)

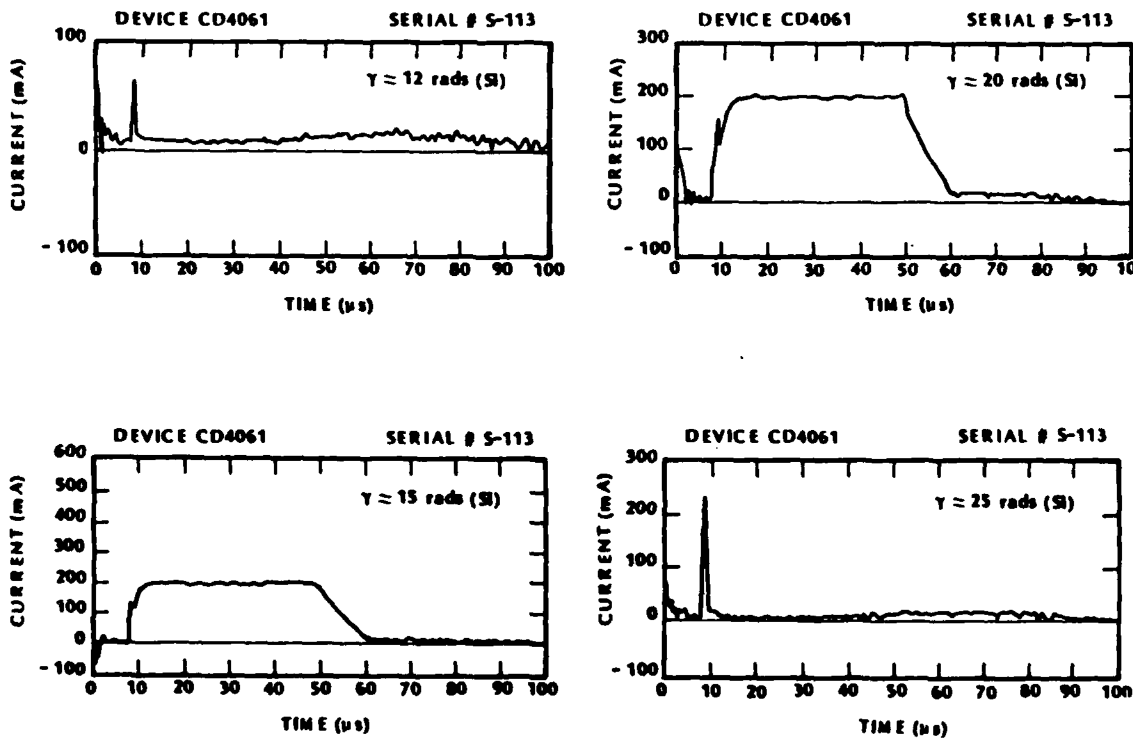


Figure 4. Latchup window behavior for the CD4061-CMOS RAM, $V_{DD} \approx 10$ volts (CD4061AD, Lot 049)

Device number	Lot	V_{DD} supply volts	Window	Dose range for* latch threshold R (Si)	Dose range for* no latch threshold R (Si)
P1	7652	10.6	no	5 - 10	-
		8.6	yes	5 - 16	18 - 23
		7.5	yes	12 - 15	15 - 19
Q	7653	10.0	no	11 - 13	-
		8.4	yes	11 - 13	17.9 - 18.4
[illegible]	7652	10.4	yes	13 - 16	21 - 29
P1	7653	10.4	yes	12 - 15	21 - 24
Q3	7652	10.4	yes	13 - 15	18 - 26
J2	869	10.4	no	-	-
J4	869	10.4	no	-	-
S112	7651	10.4	yes	12 - 16	20 - 27
S113	7651	10.3	yes	17 - 18	20 - 25
S114	7651	10.4	yes	14 - 15	18 - 19
		10.2	yes	15 - 17	17 - 17.5
S115	7651	10.2	yes	14 - 16	18 - 21

*The two values for each threshold indicate the range in which the threshold occurs.

Table 3. Summary of latchup window results for CD4061 devices (P.W. ≈ 70 ns)

Device number	Lot	V_{DD} supply volts	Window	Dose range for* latch threshold R (Si)	Dose range for* no latch threshold R (Si)
P1	719	10	no	-	-
P2	719	10	yes	144 - 170	197 - 200
P4	719	10	no	-	-
P5	719	10	no	-	-
P6	719	10	no	-	-
P7	719	10	yes**	321 - 374	643 - 760
P8	719	10	no	-	-
P9	719	10	no	-	-
J1	123	10.4	no	-	-
J2	123	10.4	no	-	-
J3	123	10.4	no	-	-
J4	123	10.4	no	-	-
[illegible]	7939	10.3	no	-	-
D4	7939	10.3	yes	401 - 403	407 - 418
CR1	127	10.4	no		
CR2		10.4	no		
CR3		10.4	no		
S2	7705	10.4	yes	145 - 206	820 - 1030
S3	7705	10.4	yes	215 - 329	579 - 680
S4	7705	10.2	no	144 - 210	

*The two values for each threshold indicate the range in which the threshold occurs.
**This device had multiple windows.

Table 4. Summary of latchup window results for CD4094 devices (P.W. ≈ 70 ns)

Table 4 is a summary of the results for all the CD4094 devices tested in this program. For some of the devices, it was necessary to raise the bias voltage a few tenths of a volt to achieve latchup. It should, however, be noted that the test cell was not temperature-controlled for these tests. The test cell temperature was found to have varied a few degrees for these tests, and therefore could account for the required higher applied voltage to achieve latchup.

SUMMARY

All device types tested exhibited latchup windows; however, there were some unusual results observed. These were: (1) multiple windows, (2) disappearing windows, and (3) window creation.

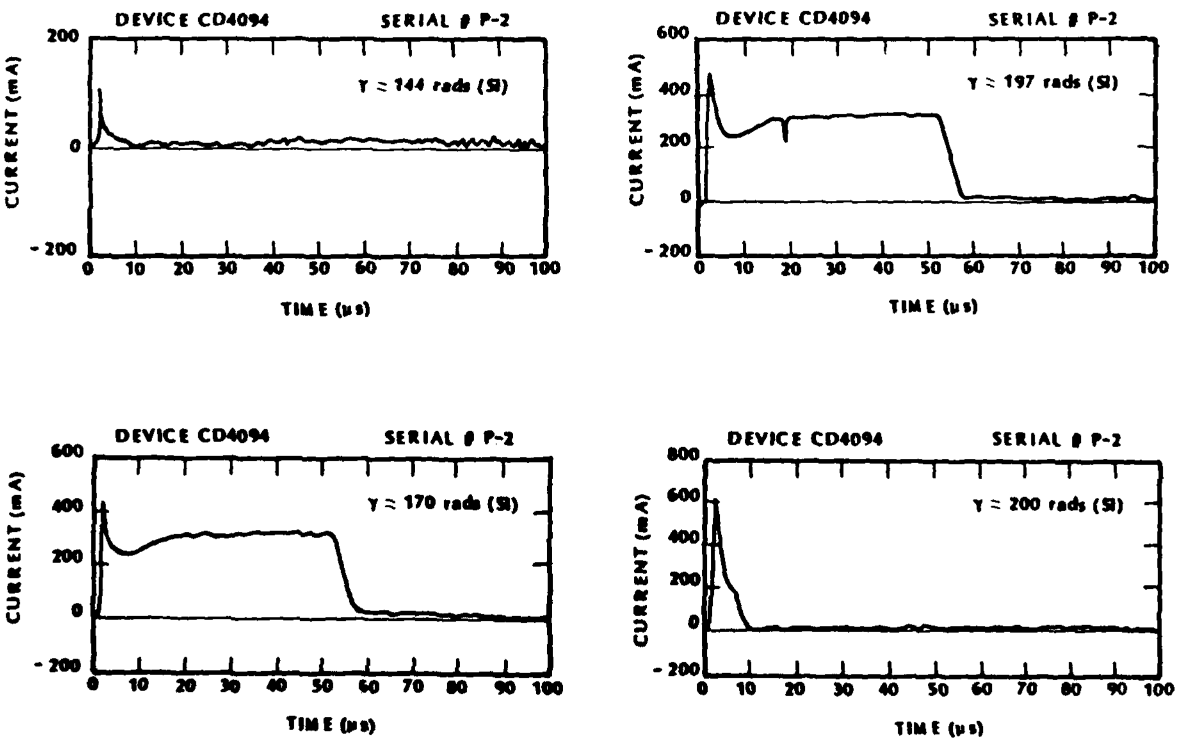


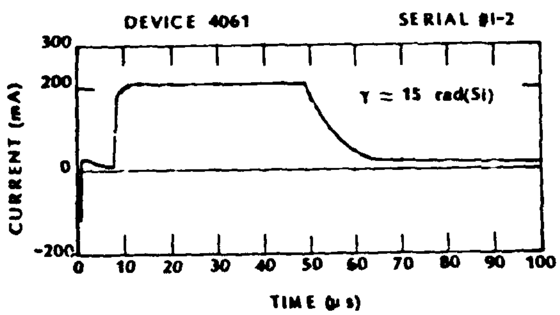
Figure 5. Latchup window behavior for the CD4094-CMOS shift register, V_{DD} ≈ 10 volts (CD4094BD, Lot 923)

At least one device in the test had multiple windows. That is, at least two regions of latchup were bracketed by regions of no latchup. These data are shown pictorially in Figure 6. How common this phenomenon may be is not known, since the experimental design searched for the existence of a latchup window and was not designed to look for multiple windows. Only in a few cases was the test continued after a single window was found and verified.

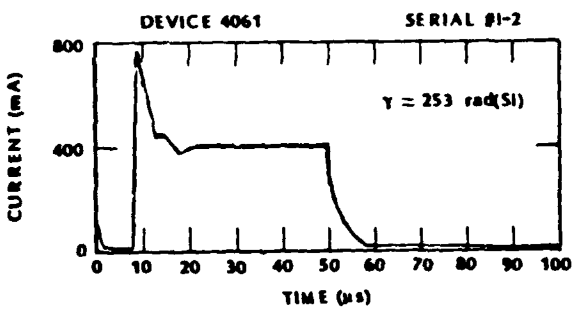
In a few cases some difficulty was encountered in characterizing the latchup window. Several pulses of the Linac at the same target dose did not always result in latchup. The explanation of this anomaly may be that the device would have a latchup window extremely narrow in dose. One can see from Figure 6 that a latchup window can be extremely small. Therefore, slight variations in Linac pulse geometry may put the test outside of the latchup window range.

On some devices, two latchup regions were found. One region was the latchup window range itself; the other was a "permanent" latchup which extended beyond the highest dose rate that could be produced during the test. The latch at the the higher dose rate range, in general, had 2 to 3 times larger "on" current than the current within the window range. Figure 7 is an example of this kind of behavior.

Figure 7 displays tracings of the power supply current for a device tested in both latchup ranges. Figure 7(a) is the typical response within the latchup window range, while Figure 7(b) is the "permanent" latchup response. The fact that the on currents are different (~ 200 mA in the window range; ~ 400 mA for the permanent latch) may indicate that different paths are involved for the two latchup regimes.



(a) Latchup window range



(b) Permanent latchup range

Figure 7. Multiple window ranges for CD4094, device no. I-2.

On some devices, it was possible to create a latchup window. In at least three cases, a latchup window was uncovered by lowering the applied bias to the test device. When the bias was reduced, the dose rate threshold for the permanent latchup range increased. On the other hand, the dose rate thresholds for the latchup window seemed to be relatively less sensitive to the applied bias. At a higher applied voltage, the permanent latchup threshold may have been lower in dose rate than the latchup window threshold, thus masking the window. At a reduced applied voltage, the permanent latchup threshold would increase to a dose rate level much higher than the latchup window range, thus uncovering the window.

This program tested 3 CMOS device types for latchup windows. These windows were found and documented. Data were taken to clearly demonstrate the existence of the windows by documenting the dose rate range where latchup occurred. At the present time, no explanation of the latchup window phenomenon is offered, however, future work will be initiated to investigate the physics of the phenomenon.

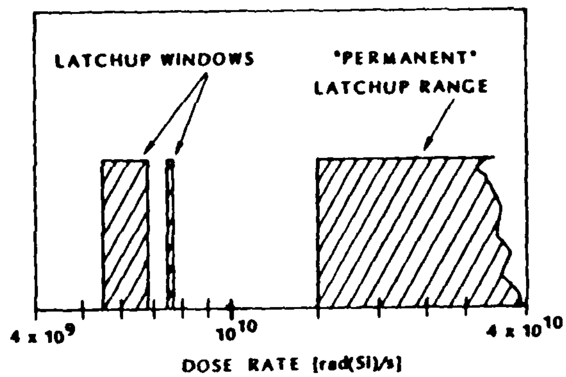


Figure 6. Latchup behavior for the CD4061-CMOS RAM, V_{DD} = 10 V.

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4. J. Azarewicz and W. Hardwick, "Latchup Window Test Report," JAYCOR Report No. J200-82-377/2249, February 1982.

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ATTN: DRSEL-NL-RO, R. Brown

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ATTN: WSSB, R. Shay

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ATTN: Code 311A, J. Adolphsen
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ATTN: Code 5301, G. Kramer
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